Comparison of Physical Gate-CD with In-Die At-Speed Non-Contact Measurements for Bin-Yield and Process Optimization

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Abstract & Overview

The timely assessment and control of process induced performance variability, especially in advanced volume manufacturing, is increasingly recognized as a key factor for the successful productization of advanced integrated circuits[1]. A novel non-contact, in-die, at-speed, performance-based metrology (PBM) technique[2] has previously been introduced that provides a high-speed metrology system suitable to ascertain the variability signature of product-representative performance metrics from manufacturing lines.

This paper reports the process-induced, systematic, in-die, and cross-wafer performance variability from a controlled 65nm technology lithography experiment (dose-exposure and trim-etch) utilizing the PBM technique, noted above. The "nominal" 65nm product lithography condition wafers are compared with those from the experimental split wafers to obtain the performance sensitivity (by direct measurement) of the transistor's "effective" channel length (L_{EFF}). These results are correlated to and compared with the physical gate-CD measurements from the same wafer sample (die/structure) locations.

The results clearly indicate that the measured variation in the physical gate CD does not fully account for the significantly increased performance variability observed for the reduced channel length CMOS devices. The performance results and variability analysis of the adjusted process conditions (general technology platform improvements) are complemented with comparisons to PBM performance and variability results from early-development phase product silicon of this technology. These results clearly indicate that tight control of gate-CD, while still of critical importance, is insufficient to account for the large increase in performance variability observed experimentally. Moreover, the results suggest that the gate-CD influence on the transistor's performance is being overtaken by other key structure (sidewall) and doping (profile, activation, and proximity) features of the device that are responsible for critical "electrical" channel length.

Summary of Results *(abridged)*

[1] Kelin J. Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Wei-kai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, and Keith Zawadzki, "Managing Porcess Varaition in Intel's 45nm CMOS Technology", *Intel technology Journal*, vol.12, no.2, pp. 93-109, 2008.

Fig. 1 illustrates a typical PBM test structure, comprised of a differential ring oscillator (RO) scheme to suppress random local process and device variations. The two ROs – one using standard 60-nm gate length (drawn) inverters, and the second built with the same number of inverters but with longer length 100-nm gates – are electrically integrated with, and powered by, a single photodiode structure. Measured simultaneously, the output frequency of each differential RO is depicted on the spectrum analyzer's signal-strength versus frequency plot and is consistent with the expected performance of a given inverter design; the lower operating frequency is from the longer gate-length inverter and the higher frequency is from the shorter gate length inverter design. It will be shown in the paper that the standard gate RO, with its shorter-gate length, is more susceptible to process-induced variations than its longer-channel counterpart.

Fig. 2 shows PBM performance measurements taken along the diameter of the two lithography split wafers (*nominal* and increased gate-etch trim). The *nominal* production wafer results are marked with *diamonds* and data from an etch-trim wafer, in which the entire wafer was exposed to an extended gate-poly etch, is marked with *triangles*. The left pane graph shows the PBM results for each wafer and associated RO gate channel-length type. The right pane shows physical gate-CD measurements for the same reticle locations, where the physical CD values of the etch-trim wafer indicate a reduction of ~ 3.6 nm from their nominal value. The results demonstrate that the expected performance shift due to the reduction of the gate channel length does not explicitly track he reduction of the physical gate length.

Conclusion

We present results for an in-line, non-contact technology to measure in-die (active product) product performance variability. These results indicate that well controlled physical gate-length is no longer the only or the dominate determining factor causing performance variability, (and more importantly bin-yield) for advanced products. The results show that both electrical and physical process important factors that influence the transistor's gate structure need to be tested and measured electrically.
These electrical performance structures are typically evaluated in the in the product scribe region), but the correlation to the in-die circuit behavior is diminishing, thereby providing decreasing visibility to product performance at the end-of-line. Costly and time consuming alternatives include send-ahead wafers or specially designed metal connection masks to obtain in-die circuit and end-of-product performance behavior. However, PBM's in-die, at-speed characterization of product-representative circuits can complement or potentially eliminate the need for these disruptive and non-representative measurements by providing an early, real time, non-contact, measurement capability for each product.

Figure 1: Differential construct monitors a control and a sensitive circuit

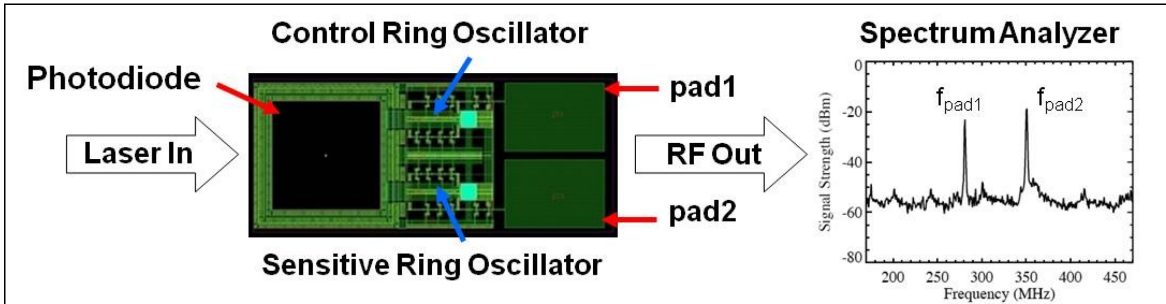

Figure 2: Wafer Diameter Scan Comparisons RO *(Performance vs. Gate CD)*