

In-Line Non-Contact Measurement of Process Induced In-Die Parametric Variability

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Biography

Dr. Vickers is the co-founder and CTO of tau-Metrix. He co-founded Optonics Inc., a design/diagnostics and FA company, and was its CTO up to its acquisition by Credence Systems in 2003. He received his doctorate from UC Berkeley in Physics.

Abstract

We describe a non-contact method of monitoring across-wafer and in-die product performance. Non-contact performance data collected from active test structures placed throughout a product die of a 65-nm volume manufacturing run with controlled lithography experiments is compared using standard physical CD measurements. Two non-standard wafers – an etch-trim wafer and a dose-exposure wafer – provide controlled processing variations to monitor resulting performance variation. We demonstrate that gate-CD measurements cannot account for the observed performance variability.

Introduction

*Metrology axiom*¹: “You can’t control what you don’t measure.”

Monitoring and controlling cross-wafer (intra-die) and in-die (inter-die) process induced variability^{2,3} has been recognized as

an increasingly critical factor for successful commercialization of high performance integrated circuit products^{4,5,6}. There is a need for in-die product-centric measurement techniques to complement traditional physical and parametric measurement and test techniques. Direct, non-contact, in-line performance measurements performed in the active area can fill this gap. Physical metrology and scribe parametric data remain important, but early, continuous, and statistically representative performance data is required to manage and improve process control without impacting wafers in the manufacturing line.

We introduce a performance based metrology (PBM) technique that can be implemented on product wafers in a high-volume manufacturing environment. The technology is non-contact and enables measurements of active test structures that can be placed anywhere in a reticle, including within product die, and used to measure performance variation. The measurement cells are independent structures and require no additional power or

“Variation”, *Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED) 2007*, pp. 15-20.

⁴ A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N. Le, P. Lindo, A. P. Mahorowala, H.-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas and H. Utomo, “Improving the Power-Performance of Multicore Processors Through Optimization of Lithography and Thermal Processing”, *Proc. of SPIE*, vol. 6521, pp. 65210K, 2007.

⁵ B. Nikolic, L.T. Pang, “Measurements and analysis of process variability in 90nm CMOS,” *Proc. 8th International Conference on Solid-State and Integrated Circuit Technology*, Shanghai, China, October 23-26, 2006. (invited), pp. 505-508.

⁶ Sharad Saxena, Christopher Hess, Hossein Karbasi, Angelo Rossoni, Stefano Tonello, Patrick McNamara, Silvia Lucherini, Seán Minehane, Christoph Dolainsky, and Michele Quarantelli, “Variation in Transistor Performance and Leakage in Nanometer-Scale Technologies”, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 55, no. 1, pp. 131-143, Jan. 2008.

¹ Anonymous.

² Kelin J. Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Wei-kai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, and Keith Zawadzki, “Managing Process Variation in Intel’s 45nm CMOS Technology”, *Intel technology Journal*, vol.12, no.2, pp. 93-109, 2008.

³ Duane S. Boning, Karthik Balakrishnan, Hong Cai, Nigel Drego, Ali Farahanchi, Karen Gettings, Daihyun Lim, Ajay Somani, Hayden Taylor, Daniel Truque, Xiaolin Xie,

test connections. The user's product-like active circuits⁷ provides a true indication of end-of-line performance that can be obtained at any process step after transistor connectivity (typically M1) up through final metals, as long as there is optical access at the time of the measurement.

The PBM results demonstrate the technique's ability to identify subtle shifts in the process conditions, such as fine tuning the device technology (RTA, film deposition, CD control, etc.), which influence the predominate, performance-critical effective gate length (L_{EFF}) of the transistors. Non-contact switching performance measurements were performed directly within the product area of a multi-product wafer (MPW) to assess in-die performance and variability. Although the specific wafers discussed here were pulled early from the manufacturing line to complete the corresponding contacted testing for verification of the non-contacted results, there was no other requirement to treat these as sacrificial-test wafers, nor was there any special processing other than the lithographic split run for the etch-trim and dose-exposure matrix results. These wafers would have required none of the aggressive and complex cleaning processes typically required to return wafers to the production flow after electrical test on product (active) die. Although the improved control of the device technology reduced the performance variability from the initial process flow, the PBM evaluation shows that even more can be gained. Because the technique measures device performance directly, no inference from physical measurements is needed and it scales favorably with the technology roadmap for advanced lithography and device structures.

Results & Data

Fig. 1 shows the non-contact PBM system architecture comprised of a) an automated measurement system (non-contact power

and signal detection) and b) the embedded on-silicon test-structures. The on-silicon product-representative circuits are developed from process and design integration libraries. The integrated non-contact test structures require neither contact probe pads nor any overhead circuitry used for traditional parametric measurements. The small-footprint of PBM's test structures (typically 10 x 30 sq. μm) can easily be accommodated by the in-die "white" space on a product. By their design and placement in the product's active area, these test structures exhibit relevant performance sensitivity to both process and design-induced variation. The design and processing of the PBM test-structures are fully compatible with standard bulk-Si and SOI processes.

Fig. 2 shows a typical PBM test structure that includes a differential ring oscillator (RO) scheme to suppress random noise and local variations. Two ROs – one built using inverters of standard 60-nm gate length and the other built using the same number of inverters of longer 100-nm gate length – are integrated with, and powered by, a single photodiode. The standard gate RO, with its shorter gate length, is more susceptible to process variations than its longer channel counterpart.

Fig. 3 shows the direct comparison between fully non-contact, optically powered PBM measurements and electrically powered probed measurements of the same test structure. Wafermaps show a very strong correlation between the non-contact and probed data sets.

Fig.4 shows measurements taken along the cross-notch diameter from two wafers. Data from a *nominal* production wafer is drawn using diamonds, while data from an etch-trim wafer, in which the entire wafer was exposed to an extended poly etch, is drawn using triangles. The left panel shows PBM measurements for each wafer and RO type. The right panel shows physical gate CD measurements for the same reticle locations, with CD values from the etch-trim wafer reduced by about 3.6 nm from their nominal value.

⁷ Mark B. Ketchen, Manjul Bhushan, "Product-representative 'at speed' test structures for CMOS characterization", *IBM Journal of Research and Development*, vol. 50, no. 4/5, pp. 451-468, 2006.

As expected, the short-channel RO oscillates faster, and suffers more across-wafer variation than its long-channel RO counterpart. Data from the etch-trim wafer, in which gate channels were further reduced from their nominal values through additional poly etch, show faster performance levels, and even more across-wafer variation, than is seen for the nominally processed wafer. Furthermore, the measured gate CD values are not seen to correlate with RO performance levels. For instance, the gate CD measurements for the etch trim wafer show a full variation range of only 1.0 nm, yet performance of the short-channel RO is seen to vary over 30% across wafer.

Conclusion

An in-line, non-contact, at-speed technique for in-die variability measurements of product-die is introduced. The at-speed differential measurements are compared to gate-CD on several wafer samples. The results indicate that controlling gate-CD, albeit critical, is not sufficient to account for the much larger deviations of at-speed variability, and the responsible process steps in “electrical” formation of the gate are strongly responsible for variability. The effect of these critical steps are ultimately measured by electrical/performance means. The PBM technology enables in-line, non-contact, in-die measurements of these effects and process steps.

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Figure 1: PBM system architecture

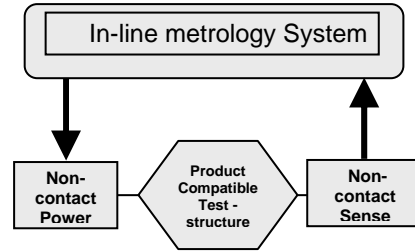


Figure 2: Differential construct monitors a control and a sensitive circuit

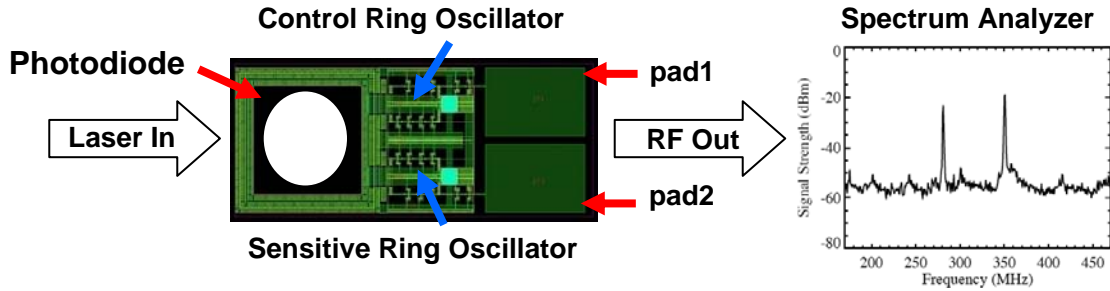


Figure 3: Probed vs. Non-Contact (PBM) Measurements (45-nm SOI, Measured at M-2)

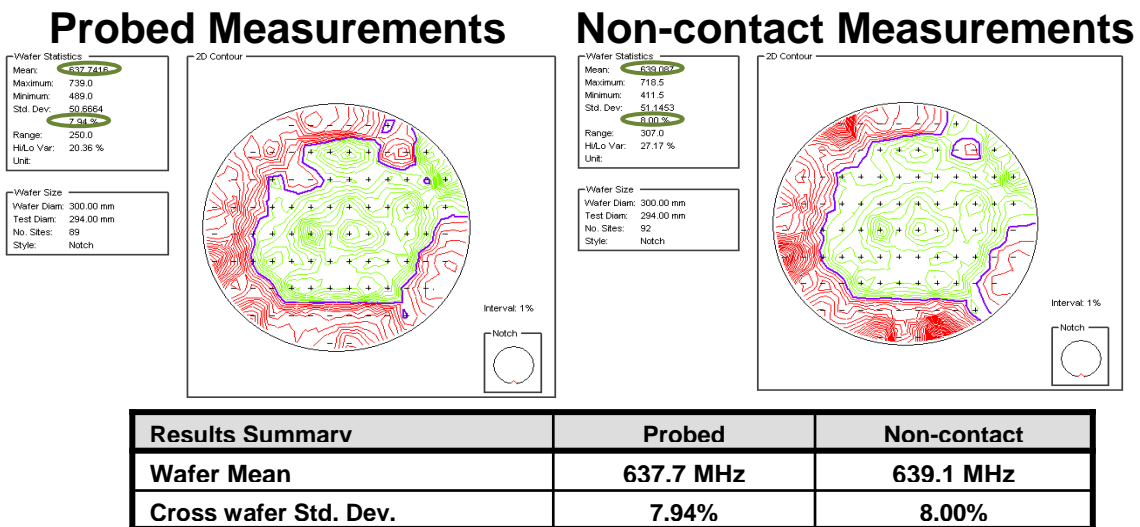


Figure 4: Wafer Diameter Scan Comparisons RO (Performance vs. Gate CD)

