Comparison of Physical Gate-CD with In-Die At-Speed Non-Contact Measurements for Bin-Yield and Process Optimization

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Abstract

We report on a performance-based measurement (PBM) technique from a volume production 65-nm multi-product wafer (MPW) process that shows far more sensitivity than the standard physical gate-length (CD) measurements. The performance (the electrical "effective" gate length, L_{eff}) variation results measured by PBM can NOT be explained alone by CD (physical gate) measurement and show that the non-destructive (non-contact) PBM is able to monitor and control at first-level of electrical connectivity ($\geq$M1), the bin-yield determining in-die variation that are NOT captured or realized by physical CD measurement. Along with this higher sensitivity, we also show that the process-induced variation (excursion) has a distinct signature versus "nominal" expected behavior.

Keywords

Non-contact, in-die performance based metrology, process-induced variability, critical physical gate length (CD), and effective channel length (L_{eff})

Introduction and Overview of the Results

The timely assessment and control of in-die process induced performance variability, especially in advanced volume manufacturing, is increasingly recognized as a key factor for the successful productization and high yield, in particular final performance dependent bin-yield, volume production of advanced integrated circuits[1, 2, & 3]. A novel non-contact, in-die, at-speed, performance-based metrology (PBM) technique[4] has previously been introduced that provides a high-throughput metrology system suitable to ascertain the performance (i.e. speed, leakage, power …) variability signature of product-representative performance metrics from manufacturing lines.

A brief overview of PBM non-contact system architecture and the differential (two) ring-oscillator technique to suppress random variations[5] and traditionally achieved through averaging by implementation of numerous long (numbering in the upper-tens and hundreds) invertors chains is presented. Some typical results of measuring in-die variability using non-contact PBM and its direct and strong correlation to contact (probed) measurement is presented.

We then report the process-induced systematic, in-die, and cross-wafer performance variability from a 65nm technology. The measurements are drawn from a controlled lithography/patterning experiment (trim-etch and dose-exposure) utilizing the PBM technique and compared with physically measured CD. The "nominal" 65nm product patterning condition wafers are compared with those from the experimental "split" wafers to obtain the performance sensitivity (by direct measurement) of the transistor's "effective" channel length (L_{eff}). These results are correlated to and compared with the physical gate-CD measurements from the same wafer sample (die/structure) locations.

In summary, the results clearly indicate that the measured variation in the physical gate CD does not fully account (minimal correlation) for the significantly increased performance variability observed for the physically "altered" channel length CMOS devices. non-contact, in-die PBM measurements that can be carried out as early as metal-1 (M1), of product-like ROs, is shown to be a much more sensitive indicator of the final performance measurement (bin-yield at final-performance test) than critical, and needed, but not indicative, CD physical monitoring and control. In short, it is shown that L_{eff} is a much better and direct measure and control of bin-yield. CD measurements should still complement this critical measurement.

Performance-based Measurement (PBM): Brief Overview

Figure 1a shows the non-contact measurement system/tool for powering up (in this configuration a photo-diode operating similar to a solar cell providing current/power at ~0.7 volt when powered by a visible ~400nm laser) and detecting the output signal of product-like activated and measured devices. In this configuration, the detected signals are voltage alterations picked off through capacitive coupling (non-contact) off a conductive pad. The design/circuit architecture of the product-like circuits are configured as ring-oscillators (ROs). The industry commonly uses ROs, modified and reconfigured, and product-like test structures in the scribe and in the product die[6].

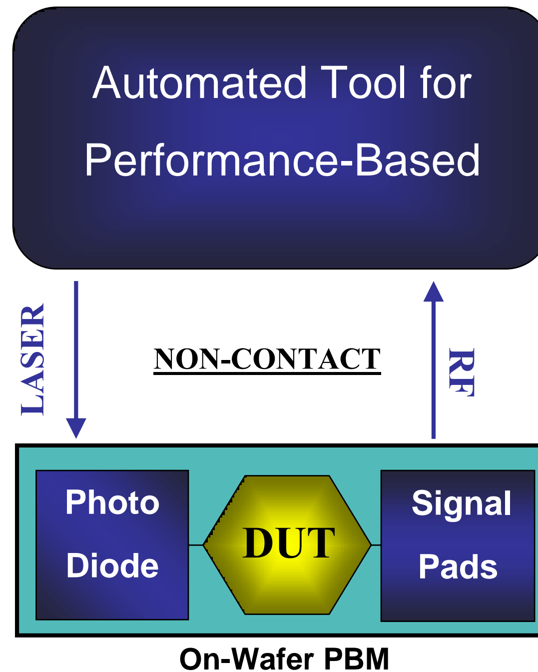


Figure 1a, Performance-based measurement (PBM) system architecture

Figure 1b illustrates a typical PBM test structure, comprised of a differential RO scheme to suppress random local process and device variations. The two ROs, in the measurements and results shown, from a 65 product design, implements the "sensitive" circuit using standard minimum CD 60-nm gate length (drawn) inverters, and the second ("control" circuit) built with the same number of inverters but with longer length 100-nm gates – are electrically integrated with, and powered by a single photodiode structure. Measured simultaneously, the output frequency of each differential RO is depicted on the spectrum analyzer's (signal-strength versus frequency) and is consistent with the expected performance of a given inverter design; the lower operating frequency is from the longer gate-length inverter and the higher frequency is from the shorter gate length inverter design. As seen in the results below, the signal/speed of the differential "long" and "short" channel ROs (point-by-point per test-structure location) correlate. In short, this correlation is achieved by the use of a common power supply (photo-diode) and the physical co-location of the "control" and "sensitive" circuits that suppress random effects.

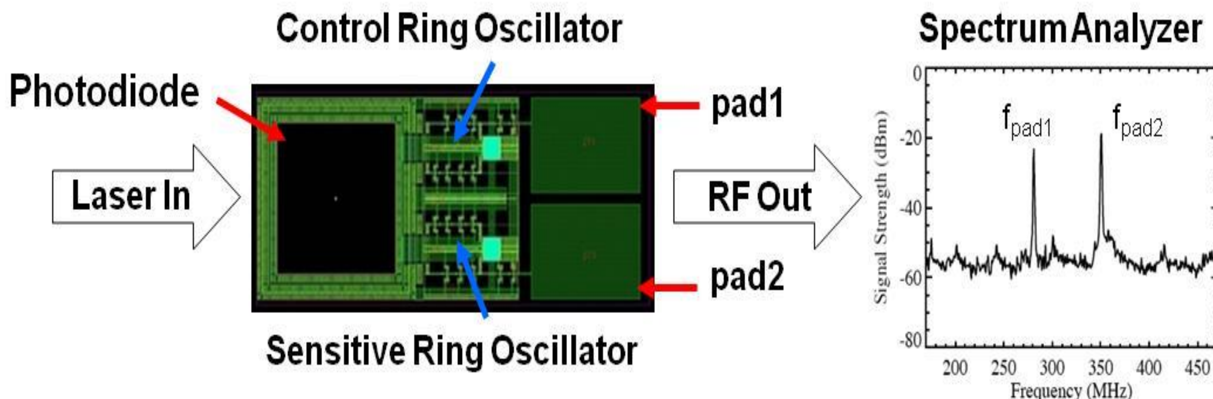


Figure 1b, Differential ring oscillators (RO)

Figure 2a compares a single non-contact PBM measurement akin to single scribe location, a very close (~1mm) to the scribe at the corner of active-die, to a multi-point (8) in-die (cross-die) product performance PBM measurement. As shown by the wafer statistics, the PBM *average variation* across the wafer match (~292.82 MHz), whereas the 1-σ standard deviation (measure of variance) shows a 57% increase. In short, the single-point (scribe-like) parametric (speed- performance) measurement is not indicative of the in-die's higher averaged variation.

Figure 2b compares non-contact PBM vs. probed (contacted) measurement on the differential RO structures and architecture on a 45nm SOI process. The wafer-maps are shown, and in particular the statistics (average and 1-σ percentage compared to the mean) are shown for each measurement technique. The non-contact PBM measurement is matched and correlates well (correlation factor > 95%) to the contacted/probed measurements. Both show the same average and, in particular the same (~8% percentage of the mean) 1-σ.

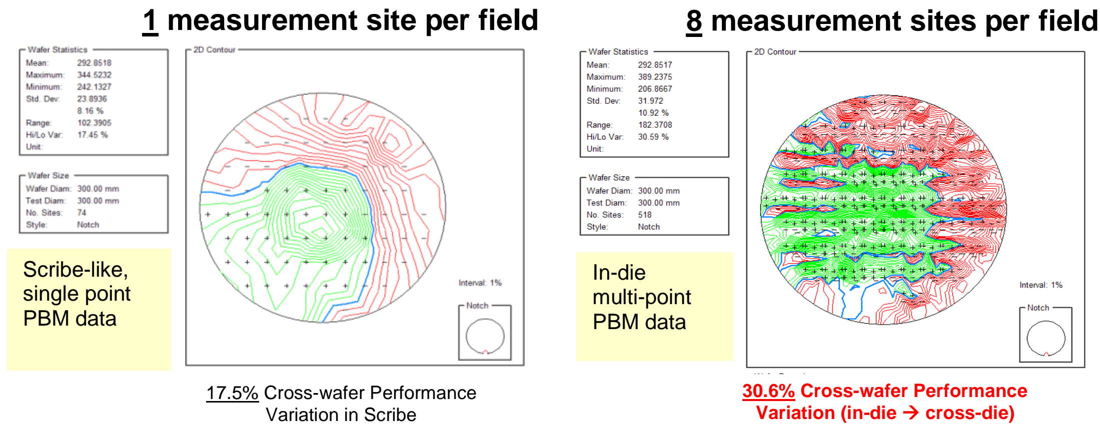
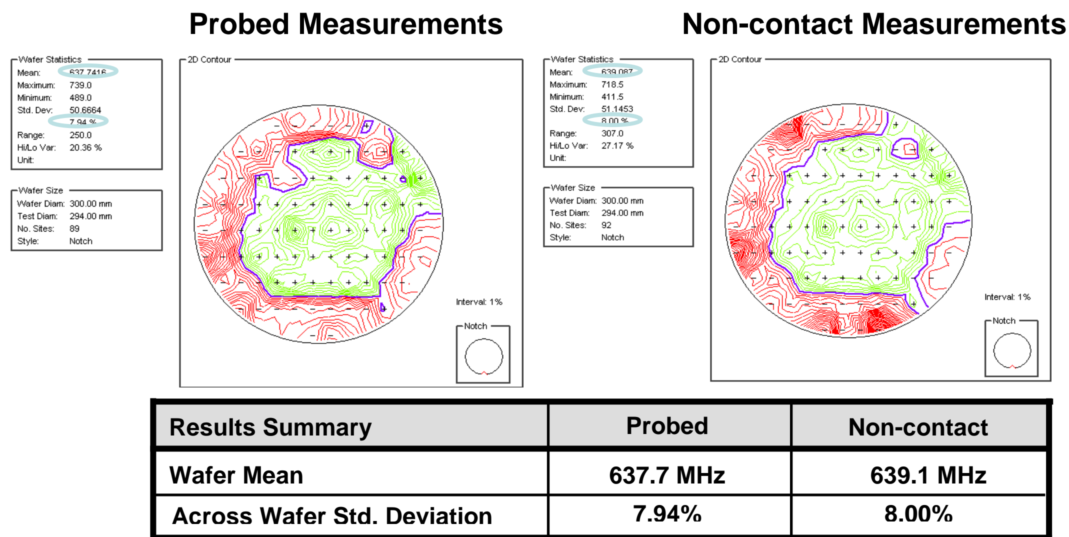


Figure 2a: PBM Measurement of Single (Scribe-like) Compared to Multi-Point (8-Point in-die)



Results Summary	Probed	Non-contact
Wafer Mean	637.7 MHz	639.1 MHz
Across Wafer Std. Deviation	7.94%	8.00%

Figure 2b: PBM (non-contact) vs. Contact (Probe) Measurement Show Very Strong Correlation (> 98%)

Experimental Results: Physical-CD vs. PBM measurements on Controlled Patterning (Trim-Etch and Striped Dose-Exposure)

Trim-Etch: Experimental Split Results

Figure 3 shows PBM performance measurements taken along the diameter of the two lithography split wafers (*nominal* and increased gate-etch trim). The *nominal* production wafer results are marked with *diamonds* and data from an etch-trim wafer,

in which the entire wafer was exposed to an extended gate-poly etch, is marked with *triangles*. The left pane graph shows the PBM results for each wafer and associated RO gate channel-length type. The right pane shows physical gate-CD measurements for the same reticle locations, where the physical CD values of the etch-trim wafer indicate a reduction of ~ (typical) 3.6 nm from their nominal value of ~62.5nm. The results demonstrate that the expected performance shift (~ 7% to 21%) does not explicitly track the reduction of the physical gate length. This indicates higher PBM sensitivity when compared to physical measured CD. In particular, the physical CD measurement and patterning although well controlled and managed do not indicate the "unforeseen" performance (end-of-line bin-yield type) performance results that determine performance yield vs. tat of physical random or systematic) variation.

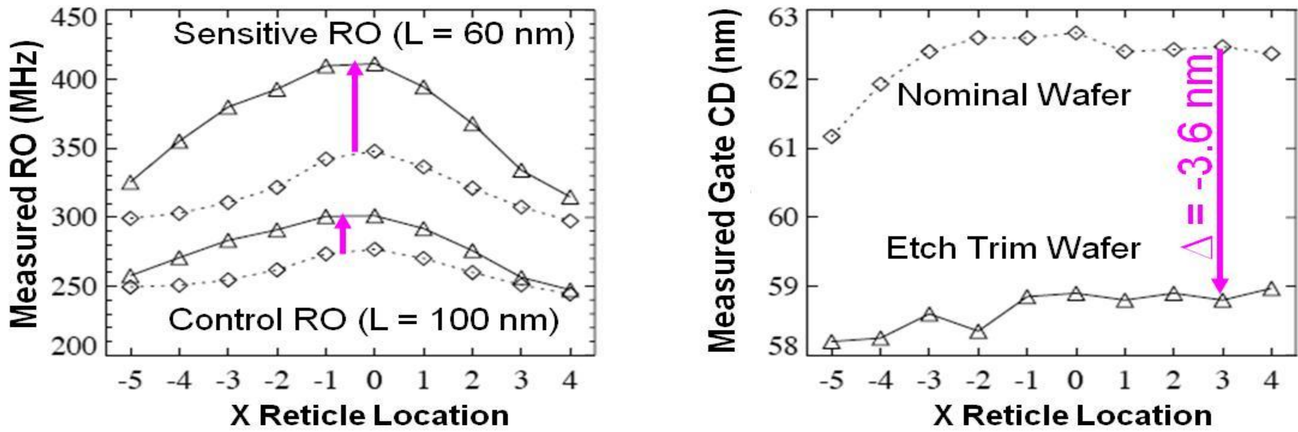


Figure 3: Wafer Diameter Scan Etch-Trimmed Wafer trend-line vs. "Nominal" Comparisons RO

Figure 4 shows that by using PBM's dual ring oscillator (RO) design technology, a new CD, predominately L_{eff}, monitoring capability is demonstrated using the relative slope behavior of the correlated differential (sensitive vs., "relaxed" in this case 60nm vs. 10nm respectively) RO operating frequencies. This new feature enables a convenient, non-contact ability to examine the CD variability behavior across wafer and, more importantly, within a product die. The immediate feedback that can influence subsequent silicon in the manufacturing line and the substantial cost saving by eliminating cleaning steps following probed data provides significant benefit during the development and high-volume product ramp cycles.

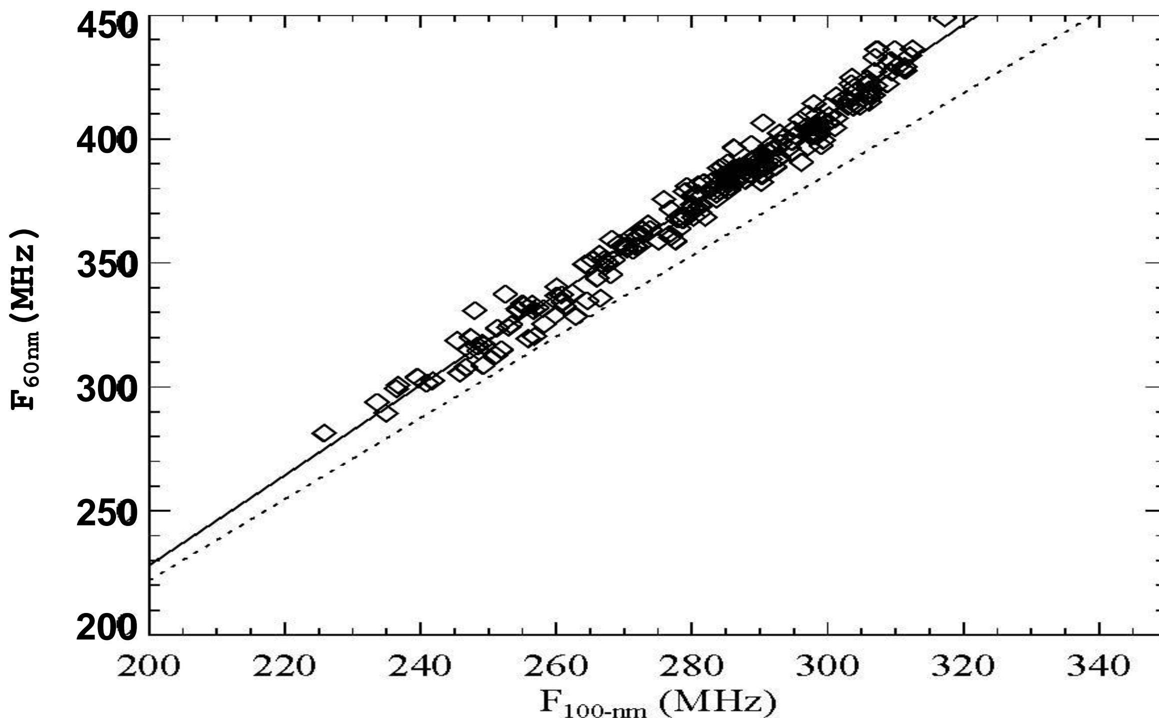


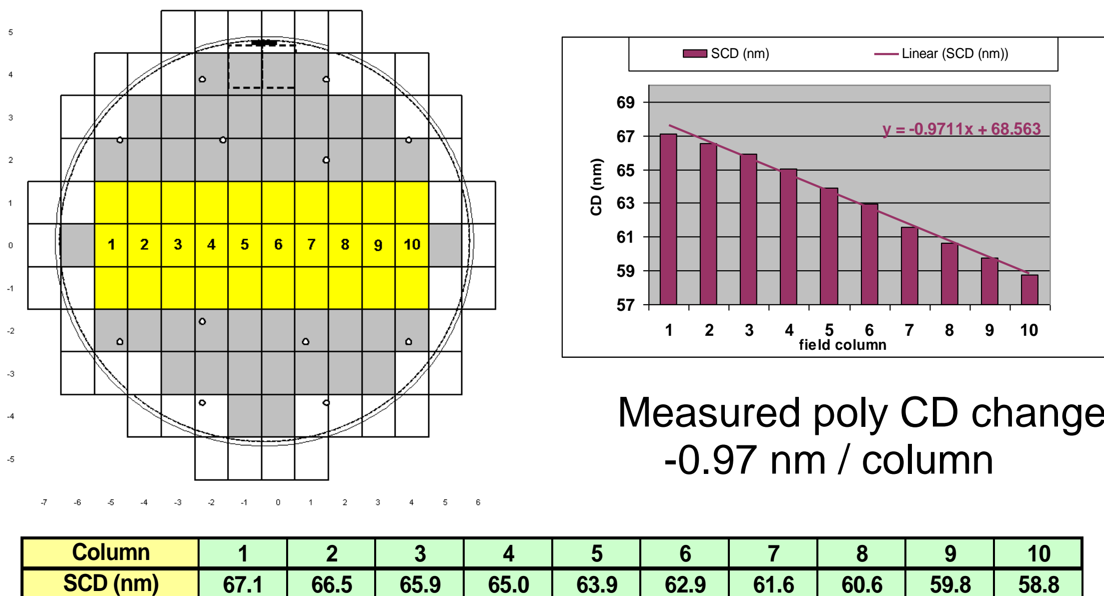
Figure 4: Wafer Diameter Scan Etch-Trimmed Wafer trend-line vs. "Nominal" Comparisons RO

As shown in Figure 4, the channel length shift was enabled by a CD trim-etch process split on the same wafer, which eliminates any wafer-to-wafer variability issues for these data that could convolute the analysis. Data for the short channel length is shown to be above the nominal channel length results, as highlighted by the shift (increased) in the slope of the least square fit (LSF) line. The correlation to the long-channel RO (where the sensitivity to the change in CD is naturally and understandably far less) is strong and, as stated previously, the increase in relative speed is well pronounced ≈ 30% for the ≈ -5% to -6% in etch-trim CD. Although the amount and range of the data is limited, the relative slope behavior of the dual RO provides the means to assess the CD and, more importantly, the L_{EFF} control of the manufacturing process.

From Figure 4 it should also be noted that the non-contact PBM technology is sensitive enough to distinguish the behavior of such a small adjustment in CDs, which could be obtained from high-resolution scanning electron microscopy[7] (HRSEM) metrology.

Striped Dose-Exposure: Experimental Split Results

The other controlled patterning experimental conditions of striped dose-exposure, shown in Fig. 5, were the physical gate (CD) measurements made on 10 columns that approximately were differentiated by physical CD by ~1nm per column. The controlled CD difference was induced by dose-exposure radiation, ranging from ~59nm to ~67nm (as shown in Figure 5), for the poly gates of both ROs (60nm "sensitive" and 100nm "control").



Column	1	2	3	4	5	6	7	8	9	10
SCD (nm)	67.1	66.5	65.9	65.0	63.9	62.9	61.6	60.6	59.8	58.8

Figure 5: Controlled Striped Dose-Exposure

Figure 5 shows the measurements and results of the nominal and controlled etch-trim experiment show that lithography (scanner) control and associated measurement is well controlled[7& 8] within ~1nm. As ultra-shallow junctions and other scaled transistor features further prevail in advanced devices, an increasing number of measurements that electrically quantify key device metrics (including performance and variability) need to be monitored throughout the manufacturing process via PBM-like characterization, physical metrology[9], and end-of-line in-die systems.

Figure 6 shows the PBM measurements of different structures in CD induced by the varying dose-exposure "extremes" vs. "nominal" trend-line. The short (-5nm, and shown as "rectangle") and long (+5nm, and shown as "triangles") CD fall to different side of "nominal" line, respectively fast (above) and slow (below) the "nominal" wafer line. Again PBM performance (speed) higher sensitivity is demonstrated and the 'spread" (distribution) is uneven (higher for the faster-shorter CD and smaller ("tighter" for the slower-longer CD) for the two extremes provided by the dose-exposure CD.

Figure 7 shows conclusively that PBM (final bin-yield and speed-performance) does not match (correlate) site-to-site (where the CD measurements have been performed) on all 3 wafers to physical CD measurements on minimal geometries. Note the "diamond" are the nominal wafer (CD 61 nm to 63 nm), and the "triangles" represent the measurements for the etch-trim wafer (CD 58-59 nm range) and "squares" are for the striped-poly wafer (CD 58 nm to 67 nm). This lack of correlation

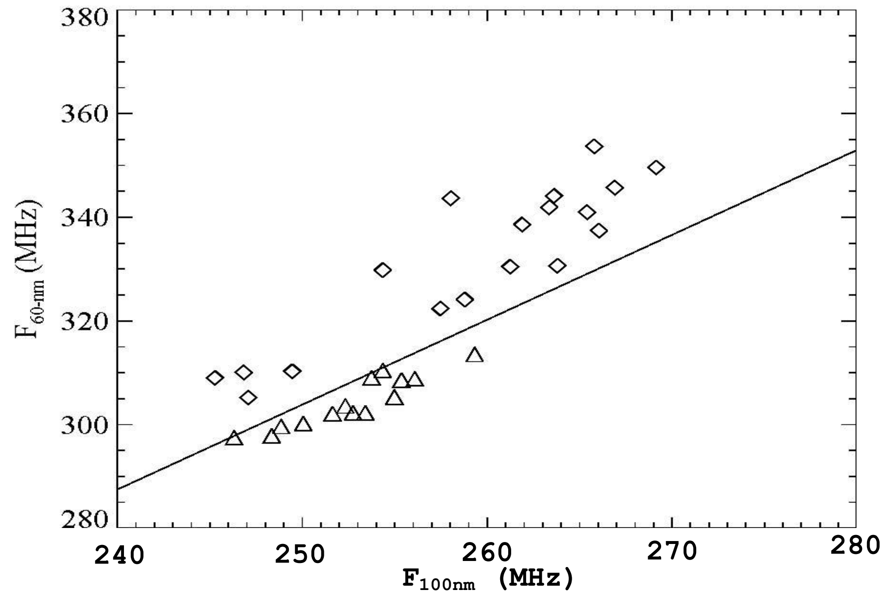


Figure 6: The (± 5nm) striped Dose-Exposure fall on two distinct sides of the "nominal" trend-line. Solid line "nominal" (~ 62.5 nm) , the "fast" -5nm (rectangle) and "slow" +5nm (triangle)

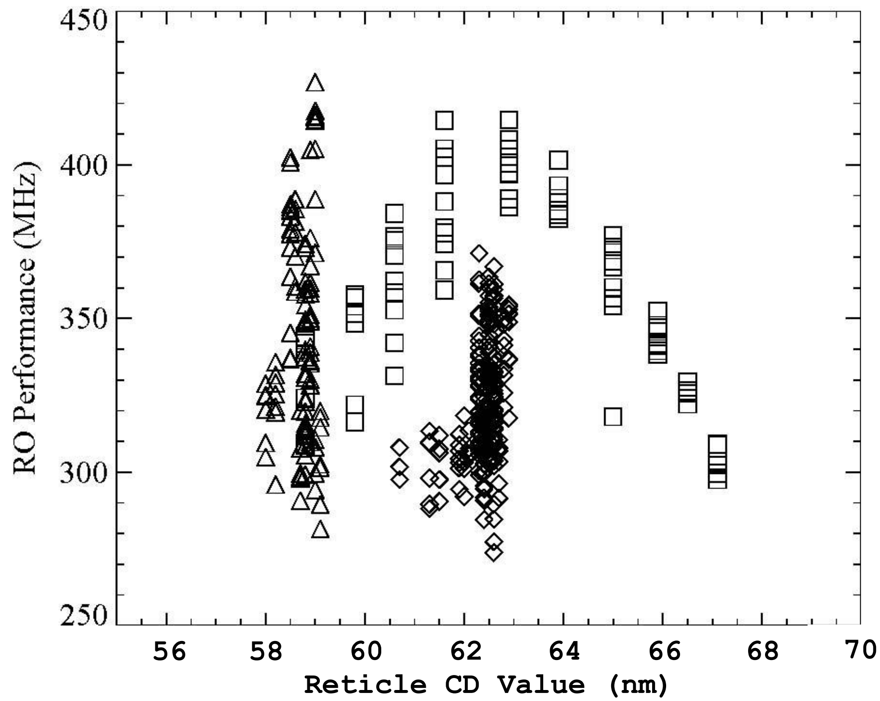


Figure 7: Diamond "nominal" wafer (CD 61 to 63 nm), Triangles etch-trim wafer (CD 58-59 nm range), and Squares striped-poly wafer (CD 58 to 67 nm)

between PBM and CD measurements indicates that CD measurements, although critical to patterning control, can not be indicative of the final performance bin-yield of product.

Summary

We present results for an in-line, non-contact technology to measure controlled in-die process induced (active product) product performance variability. These results indicate that well controlled (and measured) physical gate-length is no longer the dominant and determining factor causing performance (final yield) variability for advanced products and processes. The results show that both electrical and physical process control influence the transistor's gate structure and need to be tested and measured in tandem. In short, the ACV to litho/patterning relationship is not as strong as one would anticipate and in fact these effects were "hidden" by other sources of variability. Actually ACV sensitivity of the non-contact PBM measurements are much higher than the controlled CD changes and measurements.

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