First Look at Across-chip Performance Variation Using Non-Contact, Performance-Based Metrology

Majid Babazadeh
τ-Metrix, Inc.
Sunnyvale, CA 94089
majid@tau-metrix.com

José Estabil
τ-Metrix, Inc.
Sunnyvale, CA 94089
jje@tau-metrix.com

Bertrand Borot
Crolles2 Alliance
Crolles, France
bertrand.borot@st.com

Gloria Johnson
τ-Metrix, Inc.
Sunnyvale, CA 94089
gloria@tau-metrix.com

Nader Pakdaman
τ-Metrix, Inc.
Sunnyvale, CA 94089
np@tau-metrix.com

Wim Doedel
Crolles2 Alliance
Crolles, France
wim.doedel@philips.com

James Vickers
τ-Metrix, Inc.
Sunnyvale, CA 94089
vickers@tau-metrix.com

Gary Steinbrueck
τ-Metrix, Inc.
Sunnyvale, CA 94089
gs@stau-metrix.com

Jean Galvier
Crolles2 Alliance
Crolles, France
jean.galvier@st.com

Abstract

We report on the first non-contact, non-destructive performance measurements of embedded Ring Oscillators. Measurements are made on inside the die active area as early as Metal 1. A 90nm logic CMOS technology was used for this work. We have measured residual across-field performance variation separate from and of opposite sense to wafer uniformity. This effect cannot be extrapolated from scribe measurements.

Keywords

Across-Chip Linewidth Variation (ACLV), across-chip variation, in-field uniformity, in-line metrology, non-contact probe, embedded Ring Oscillator, DFM.

INTRODUCTION

Two wafer fab trends are dictating the need for direct understanding of across-chip performance variations: increasing lithography complexity resulting in an alphabet soup of design for manufacturing (DFM) products (OPC, RET,…); and the increasing pattern factor variation between the chip active area and scribe monitoring due to greater functional integration at the chip level for microprocessor manufacturers and to the pressure to deliver functional hardware quickly for foundry manufacturers to win business. Many logic houses routinely embed devices (typically ring oscillators) in the active area and route them so that they can be tested at Final Test as part of their yield/diagnostic strategy [1,2]. These are measured to understand in-die performance variations resulting from across-chip process variations (ACV): from photo/etch interactions, CMP dishing and erosion, and other process interactions not observed with "scribe" measurements. These techniques are not currently available to foundries: here costly test-chip only wafers are run periodically to control random and parametric defectivity as a proxy to direct in-chip measurement [3,4]. These critical variations impact chip yield increasingly with device and metal densities, particularly below 90nm. While many studies into this area focus on simulation techniques to "design" out systematic across chip variation [5], [M. Levitt, "Using Yield-Focused Design Methodologies to Speed Up Time-to-Market", presented at SPIE Microlithography 2005], we believe there is merit to making direct measurement to confirm, refine and assure that DFM techniques have worked.

This paper reports on a new technology –SILOET– used to make non-contact, non-destructive, fast measurements of embedded electrically active devices inside the chip active area. Measurement of these embedded devices upstream, as early as the first metal interconnect level ("metal zero" or M1) instead of at Final Test significantly improves time-to-action for poorly performing wafers.

PBM MEASUREMENT TECHNOLOGY

The Performance Based Metrology (PBM) concept discussed in this paper is similar to mainstream inspection/metrology technologies in that a wafer containing a metrology box is precisely positioned underneath a measurement head to collect a set of measurements. Unlike conventional optical metrology techniques, however, some of the technology "smarts" are placed into the metrology target enabling contact-less measurement and eliminating contact damage (chipping, scraping, etc.) associated with in-line electrical measurements, and greatly increasing

measurement through-put. The metrology boxes enable routine sampling of multiple locations within a field and multiple fields per wafer, typical in-line metrology requirements.

PBM deliverables are diagramed in Figure 0, and consists of a measurement tool to precisely position wafers, provide an energy beam, detect and record device electrically activity, and visualize collected data into maps, etc. and a metrology box that consists of a power circuit, a detection circuit, and the device(s) to be tested. Standard CMOS processing is used for the metrology box. Test devices can be simple structures like ring oscillators or complex structures like SRAM cells. Single or multiple test structures can be wired to a single contact-less power supply. The metrology box can easily fit into pattern fill areas (or "slop") and are typically less than 50µmx50µm. In practice, we've found that there is more real estate available for metrology boxes inside chip active area than what is typically available in the scribe.

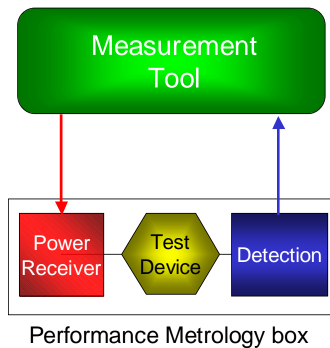


Figure 0. PBM schematic.

The PBM measurement system uses Silicon Opto-electronic Technology (SILOET): a proprietary technique based on the non-contact generation of electrical power on standard CMOS, and the detection of resulting electrically activity in test structures when connected to the power source.

The SILOET technology has six distinct advantages:
1. Measurements are based on electrical performance, not apparent line widths so they are not resolution limited and are not challenged by 65nm or 45nm technology ground rules;
2. Measurements are non-contact so wafers continue wafer processing after measurement
3. Multiple devices at the same site can be measured simultaneously;
6. Metrology boxes are small so they many be embedded throughout the flash field;
4. Measurements are direct, not model-based;
5. Measurements are very fast, collected in less than 1 sec/site.

The work in this paper was conducted on a prototype of the PBM-1000x metrology tool, a system which is commercially available.

WAFER FABRICATION

To confirm the viability of this new inspection methodology, embedded structures were co-located near multiple product geometry locations within a single-chip reticle field. Wafers have been processed using a standard 90nm (low-power dual Vt with 3.3V I/O transistors) manufacturing technology available in the Crolles2 Alliance 300mm production line. Technology features are: classical STI, gate patterning using 193nm lithography, CoSi2, CMP planarized PMD and W-plugs for contacts, 6 layer Cu metallization in a semi-line-first interconnect technology.

Metrology boxes were designed and embedded within two separate multi-product design reticles to measure the degree of performance variation across the reticle field (and wafer). The two product sets represented a typical product mix of a large field and medium field reticle as illustrated in Figure 2.

Each electrically-active metrology box depicted in Figure 2 consisted of three elements: a non-contact power generation structure; a device to be tested (buffered Ring Oscillators); and non-contact detection structures. Wafers were pulled at M1, M2 or MF for testing on a PBM-1000x prototype tool at room temperature. Results were gathered in automated runs and tabulated.

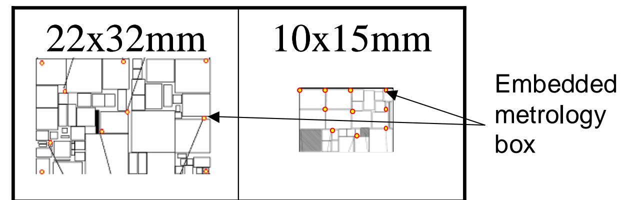


Figure 2. Distribution of embedded metrology boxes across two product reticles. There are 10 metrology boxes each in the 22x32 reticle and the 10x15 reticle. The location of each is marked with a small circle.

Wafers were measured at Metal 1 (M1) and Metal Final (MF). Data were collected on the tau-Metrix PBM-1000x. No sample preparation was required.

CMOS POWER GENERATION AND TEST DETECTION

Proprietary, small power and detection structures have been designed by τ-Metrix, Inc. (TMI) to be used in standard 90nm CMOS processing. No special masks or processing steps are required. The power and detection structures are discrete elements of the PBM target design. The structures are designed to fit in place of pattern fill, or "slop". For the

experiments reported here, power structures 35µmx35µm and 25µmx25µm were used. These structures can be physically reduced without impacting power generation or stability, but in practice are designed to be large enough to ensure simple pattern recognition-assisted placement under the PBM measurement head. The amount of current generated in the metrology box can be modulated by the measurement tool power as shown in Fig. 1 and was used to test the linearity of current generation with power.

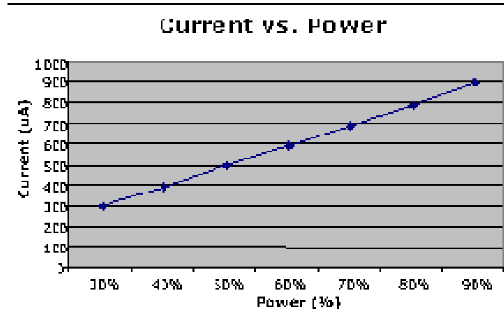


Figure 1. Current generated in metrology box vs. measurement tool power.

Stable power generation is possible and available across multiple sites within a reticle field and across the wafer. We have found power stability to be less than 0.5% under normal test conditions, and well within the precision requirement to measure across-chip and across-wafer variance.

Table 1. Power generation repeatability (~0.1%) vs. wafer uniformity (~11%).

	voltage (mV)	f(MHz)
1	730	177.4
2	730	202.8
3	728	210.3
4	730	231.4
5	731	246.7
6	731	240.8
7	732	245.2
8	731	257.3
9	731	219
10	730	182.7
11	729	188.1
12	730	215.8
13	730	234.3
14	729	250.2
15	730	237.8
16	730	261.9
17	730	249.9
18	731	238.8
Average	730.2	227.2
Variance	0.9	25.9
	0.1%	*11.4%*

Table 1 shows the results of specially designed Ring Oscillator (RO) test structures that can be powered by either a contact and/or contact-less method. Measurement of the RO frequency (in MHz) and operating voltage (in mV) across the diameter of a 300mm wafer are shown demonstrating ~0.1% power device output uniformity for 730mV operating voltage in the presence of ~11% RO performance speed variation.

ACROSS-WAFER PERFORMANCE UNIFORMITY

Figure 3 shows a typical performance uniformity map collected at M1 post copper cap using the non-contact PBM approach of this paper. A fast center/slower edge profile for the large field product run is seen. We believe this is the first published result of across chip (active area/in-die) and across wafer performance results. These results are qualitatively and quantitatively richer than that obtained from scribe parametric testing.

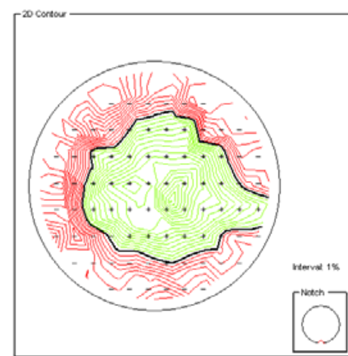


Figure 3. 300mm Non-contact performance uniformity map showing a typical fast center/slower edge profile.

Many logic manufacturers routinely embed Ring Oscillator (RO) (or more sophisticated circuitry) within their chip wire it to an I/O pad, and measure it when the chip is probed for yield at the end of manufacturing sequence. To show the validity of contact-less probing at earlier processing levels a lot was split at M1 and the rest of the lot processed until MF. Figure 4 shows that measurement of embedded RO at M1 Cap was similar to that at MF. This means similar information can be obtained much earlier in the manufacturing process flow.

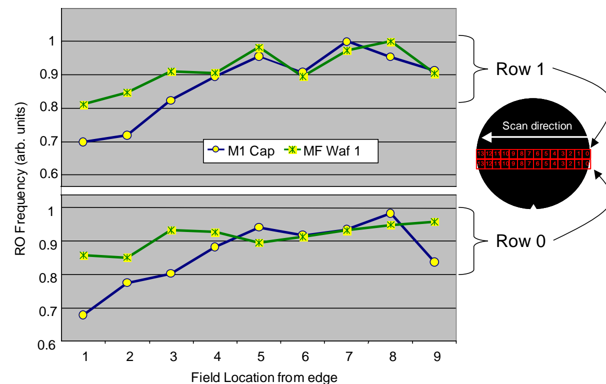


Figure 4. M1 and MF PBM measurement correspondence. (two wafers from one lot are shown).

Ten repeated measurements –with a pause in between measurements- were collected to test static precision. Typical precision results across the wafer are better than

0.5% as shown in Figure 5 where the 10 sets of non-contact measurement data are overlaid for each position within the locations in a field. Further improvements can possibly be achieved with environmental control.

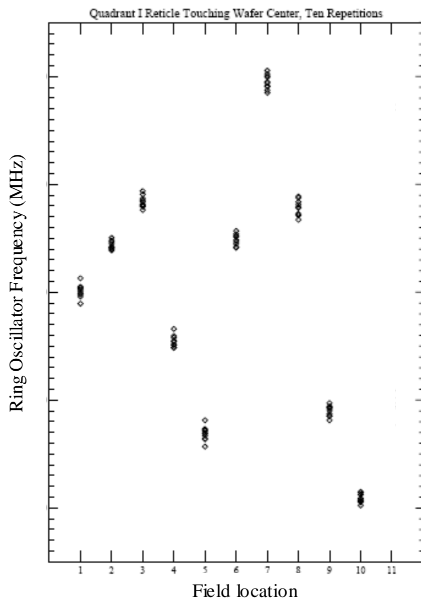
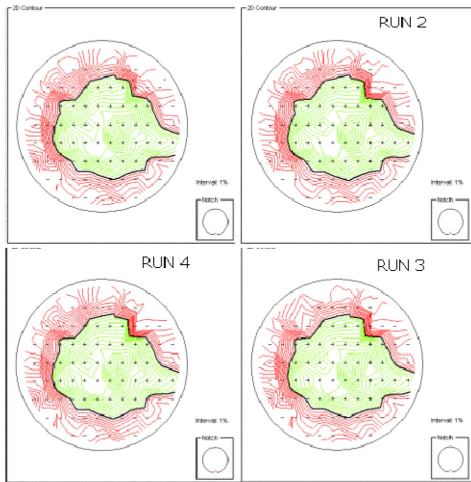


Figure 5. 0.5% measured precision across a typical reticle field.

Tight precision control is important to insure that repeatability from run-run is assured, and has been achieved as can be seen by repeated mapping of a wafer over a 24 hour period (Figure 6).



Four maps over a 24 hour period show Identical performance uniformity .

ACROSS-CHIP PERFORMANCE UNIFORMITY

Uniformity maps within the reticle field are also simultaneously collected during measurements. These measurements cannot be deduced from scribe parametric measurements with the same level of detail across the wafer. Figure 7 shows the results for the 10 fields across an entire wafer showing significant difference between from location to location within the reticle field. These differences arise from pattern factor related process steps and are surprising to see for medium size reticle field.

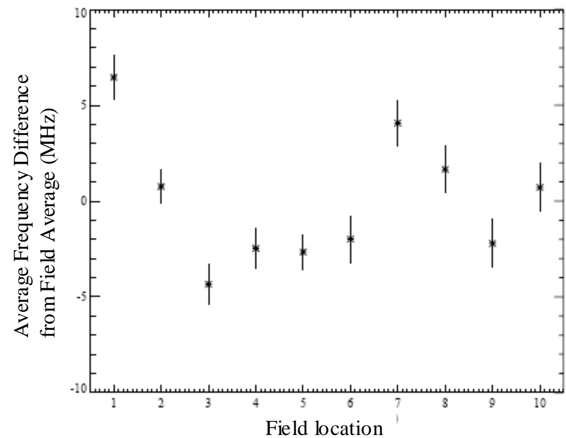


Figure 7. Across-chip variance (ACV) for a medium field size reticle.

A more revealing visualization is typical "stacked" die map is shown in Figure 8: the field perimeter is faster than the field center, a trend opposite in flavor to wafer-level uniformity trend. The magnitude of the variance from average is plotted against the in-field position showing a clear pattern. This variance is not wafer-based: it is within-die base. We believe this is the first direct observation on product wafers performance-based ACV (or ACLV as is called elsewhere). Previous studies have made similar measurements on test-wafers using full-test rectlcles [4,6].

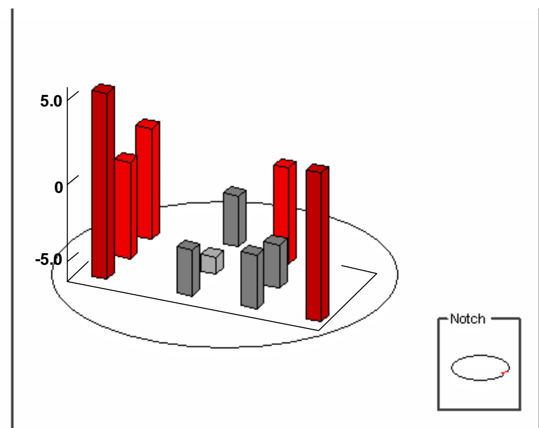


Figure 8. Across-chip variance (ACV) stacked die map showing slower center/faster perimeter.

METROLOGY CORRELATION

Excellent correlation to in-line measurement has been established. Figure 9 shows good correlation of PBM meas-

urement of RO test structures at M1 Cap (y-axis) to CD SEM measurement (x-axis). An un-intentional process split in Gate CD between two wafers is present. PBM measurements were collected “blind” (no knowledge of) to the process split and used a single recipe for both wafers.

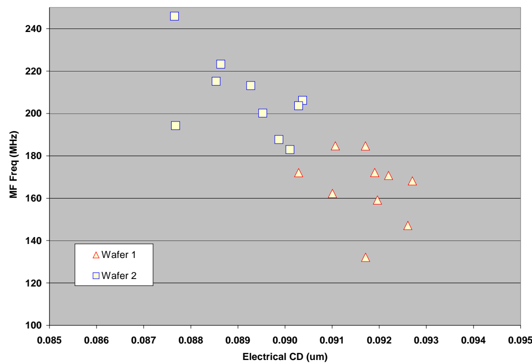


Figure 9. Good correlation between M1 Cap PBM RO and Gate CD SEM measurement.

The higher sampling frequency of PBM –at throughputs higher than CD SEM- allows for routine metrology. Two examples are presented below: Gate CD split and Gate threshold voltage (leakage). Figure 10 shows PBM uniformity maps for the Gate CD split. The higher PBM sampling (multiple measurements within a field) at comparable through put to CD SEM allow for simple process fingerprint complementary to and not possible for routine CD SEM sampling plans.

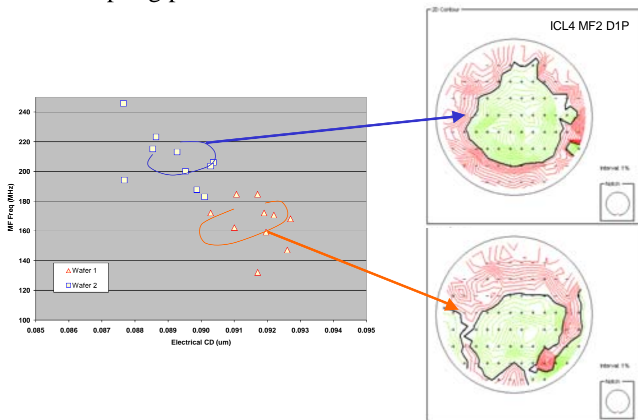


Figure 10. PBM uniformity maps (right) discern process fingerprint difference in Gate CD split.

Similarly, the uniformity signature of PBM measurement of Ring Oscillators can determine whether Gate threshold voltage variance (leakage) or Gate CD variance dominates within wafer and within die parametric performance variation. Figure 11 shows a clear correlation between PBM RO measurement and Gate parametric measurement.

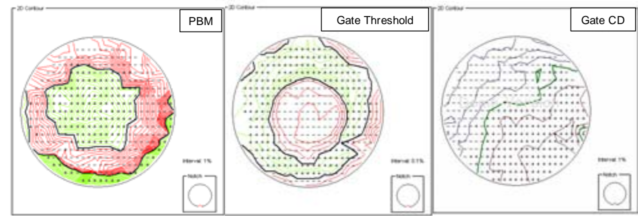


Figure 11. PBM uniformity map of RO speed at M1 (left) correlation to parametric Gate Threshold (center). Parametric Gate CD is seen not to correlate.

SUMMARY

Through the use of non-contact SILOET (Silicon Opto-Electronic Technology) we report unambiguous yield-impacting performance variances that cannot be sampled by scribe probe testing and that is typically assessed through manual, episodic, and costly destructive failure analysis techniques after Final Test. We also report measurement of within-field performance uniformity of RO’s where the wafer was center fast and the die was edge fast using the PBM-1000x contact-less metrology tool. Further investigation into the technology will focus on the types of test structures that can be manufactured to allow extraction of process and design parameters.

ACKNOWLEDGMENTS

We’d also like to thank Emmanuel Braud and Olivier Henry of the Crolles2 MPW team for their continuous support and the Crolles2 Manufacturing Line for wafer processing . We’d like also like to thank the cooperation of Wolfgang Vollrath of Leica Microsystems for technical support in data collection. We’d like to thank Tom Wong, Behrooz Yadegar, and Marc Allard from t-Metrix for their contributions.

REFERENCES

[1] Ketchen, M., Bhushan, M., Pearson, D., “High Speed Test Structures for In-Line Process Monitoring and Model Calibration”, Proceedings of the 2005 ICMTS, 2005.

[2] Stinson, J., De La Iglesia, E., “Process Parameter Extraction”, USPTO 6,353,545, April 2003.

[3] Gaither, J., Hassoun, M., “Analog signal test circuit and method”, USPTO 6,653,827, November 2003.

[4] Calderone, A., Wang, F., La, T., “Methods and Circuits for testing a circuit fabrication process for device uniformity”, USPTO 6.507,942, January 2003..

[5] Orshansky, M., Milor, L., Chen, P., Keutzer, K., Hu, C., "Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pp. 544-553, May 2002.

[6] Gonzalez-Valentin, Karen M., "Extraction of Variation Sources Due to Layout Practices," S.M. Thesis, MIT

Dept. of Electrical Engineering and Computer Science, May 2002.

BIOGRAPHY

Majid Babazadeh received his Bachelor of science in Electrical Engineering from Tehran University in 1989 and his Master of Science in Electrical Engineering from University of Southern California in 1996. Following Teradyne and n&k Technologies, he joined τ-Metrix in 2003 as Engineering Director.

Bertrand Borot graduated from Grenoble INPG in Microelectronics and Computer Science. He is currently responsible for the design of test chips dedicated to process setup and monitoring at STMicroelectronics in the Crolles2 Alliance.

Wim Doedel received his Masters degree in Chemical Technology at the Eindhoven University of Technology in the Netherlands. He is currently working for Philips Semiconductors in the Crolles2 Alliance as Industrial Process Integration manager.

José Estabil received his Bachelor and Masters degrees in Physics at Brown University. He is currently the President of τ-Metrix and was involved in the development of multiple, successful metrology products at KLA-Tencor.

Jean Galvier graduated from Montpellier ISIM in Materials Scince and Technology. He is currently working for STMicroelectronics as ramp-up Manager within the Crolles2 Alliance

Gloria Johnson received her degree in Chemistry at Reed College. She is responsible for applications development at τ-Metrix and has over fifteen years experience in metrology.

Nader Pakdaman completed his graduate studies in applied physics and electrical engineering at Purdue University and Columbia University. He is the co-founder of τ-Metrix, and co-founded Optonics in 1998, a semiconductor diagnostics company that was acquired by Credence Systems in 2003.

Gary Steinbrueck received a B.S. degree in electrical engineering from the University of Missouri at Rolla in 1968. He retired from IBM in 2002 to co-found τ-Metrix, Inc. and is currently its Chief Designer.

James S. Vickers received his Bachelor of Science degree in Physics from Purdue University, and his Masters and Ph. D. degrees from the University of California at Berkeley. He is currently the CTO and co-founder of τ-Metrix. In 1998 he co-founded Optonics, a semiconductor diagnostics company, which was acquired by Credence Systems in 2003.