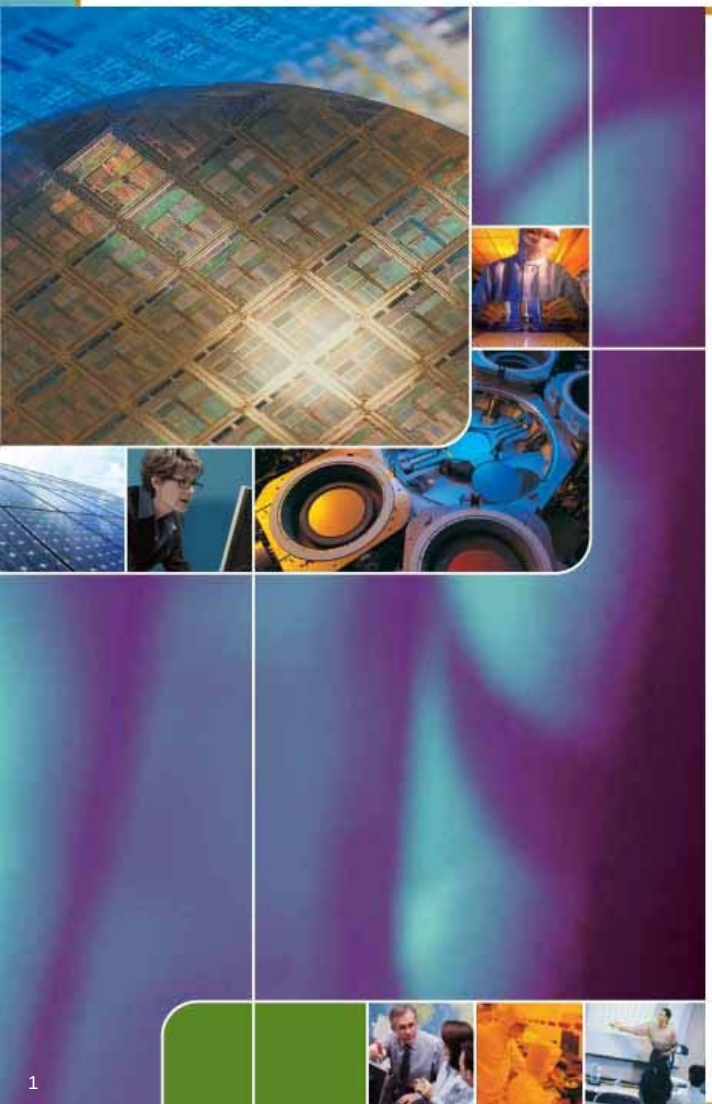
SEMI Technology Symposium (STS)



James S. Vickers, Ph.D.

τ-METRIX
Performance-based Metrology™

semi™

Authors

http://tau-metrix.com/pdf/SemiJapan_tau-Metrix_Vickers.doc

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  - Wim Doedel*
  - Bertrand Borot
  - Maxime Gatefait
  - Pascal Gouraud
  - Patricia Gros

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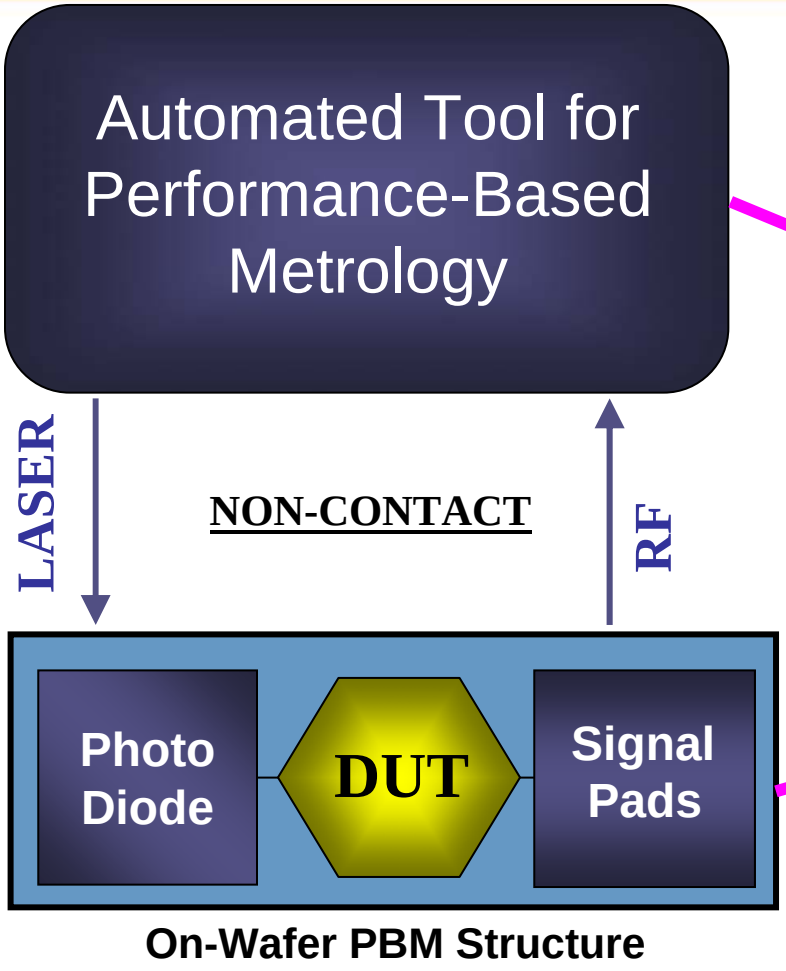
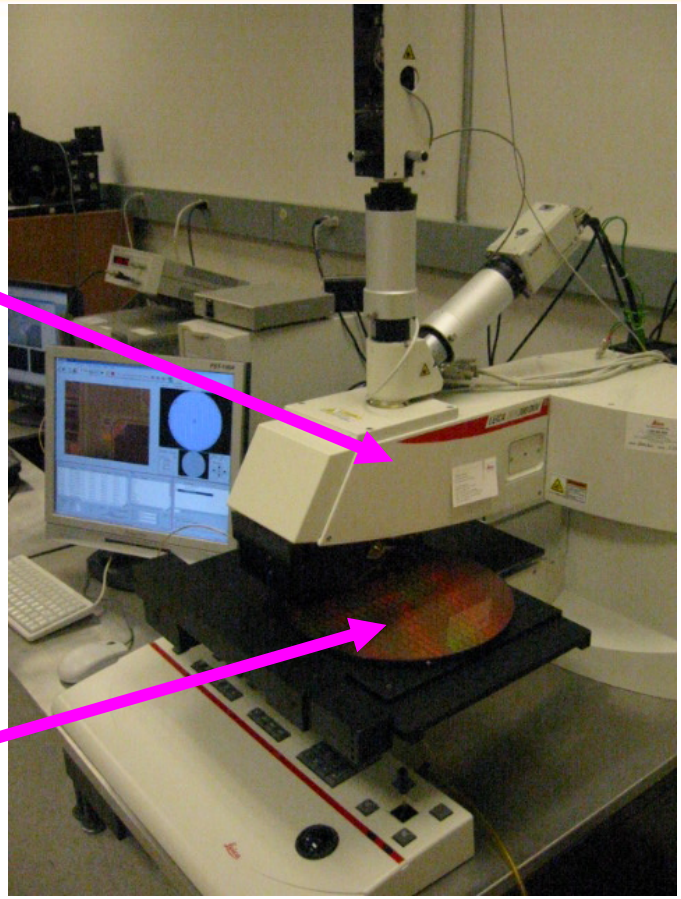
Outline

- Introduction to Performance-Based Metrology (PBM)
- Results I: Early 65-nm bulk Si process
  - Nominally processed wafer
- Results II: Improved 65-nm bulk Si process
  - Three-wafer process split
    - Nominal wafer, Etch Trim split, and Exposure split
- Summary
  - Gate CD does not correlate with final performance

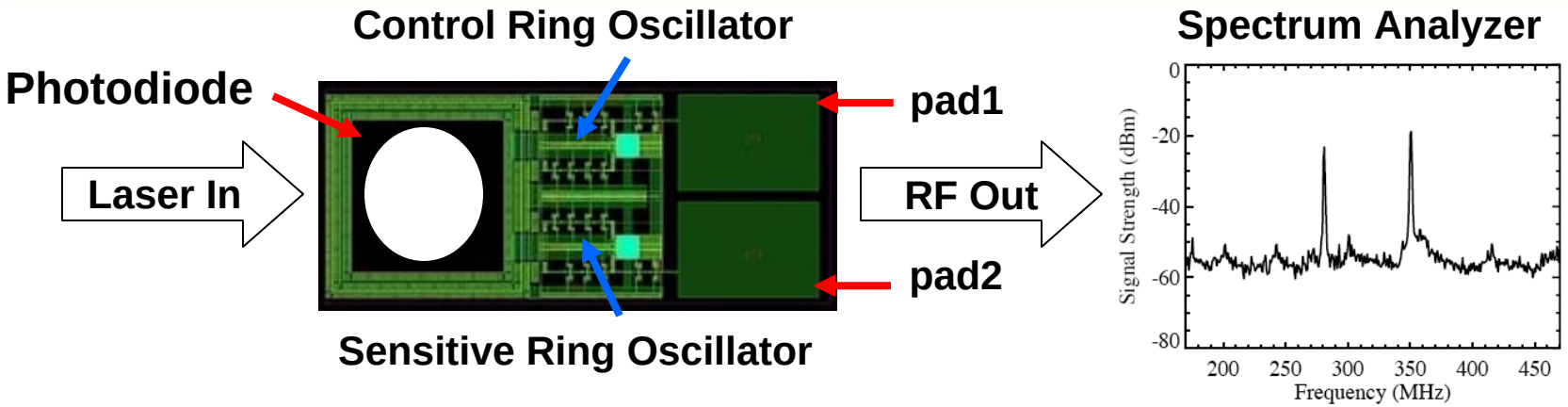
Performance Based Metrology (PBM):
Non-Contact Measurement Technique



On-Wafer PBM Structure

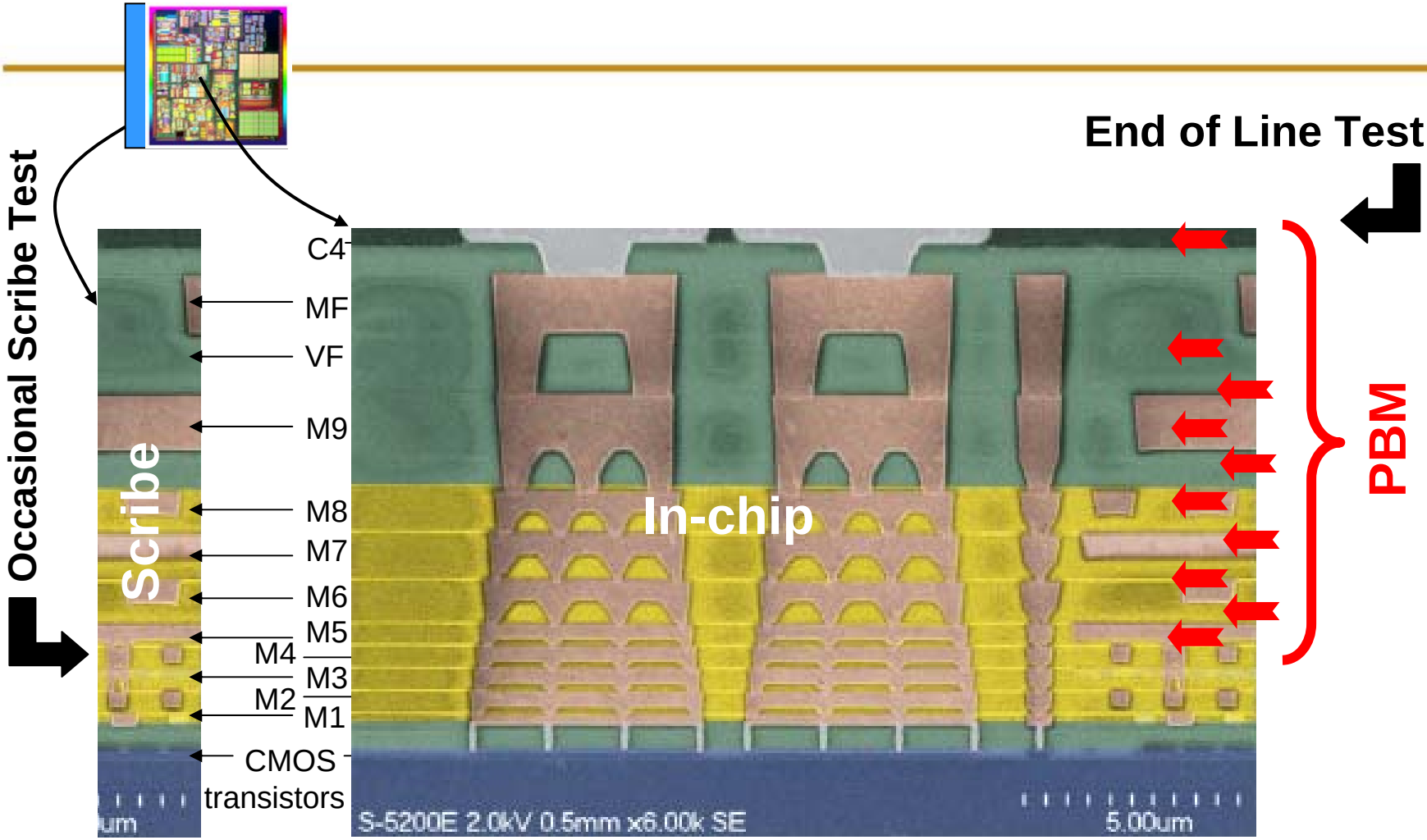


On-Wafer PBM Structure



- Small size: ~ 10 by 20 μm, can be placed in scribe or within product
- Autonomous design
  - Self powered and independent of surrounding circuitry
  - Uses standard CMOS design with normal process flow
- Differential construct monitors a control and a sensitive circuit
  - Power supply variations common to both ROs
  - Implemented INV, NAND, NOR, and customer-modified SRAM-based ROs

Scribe vs. In-Product Comparison

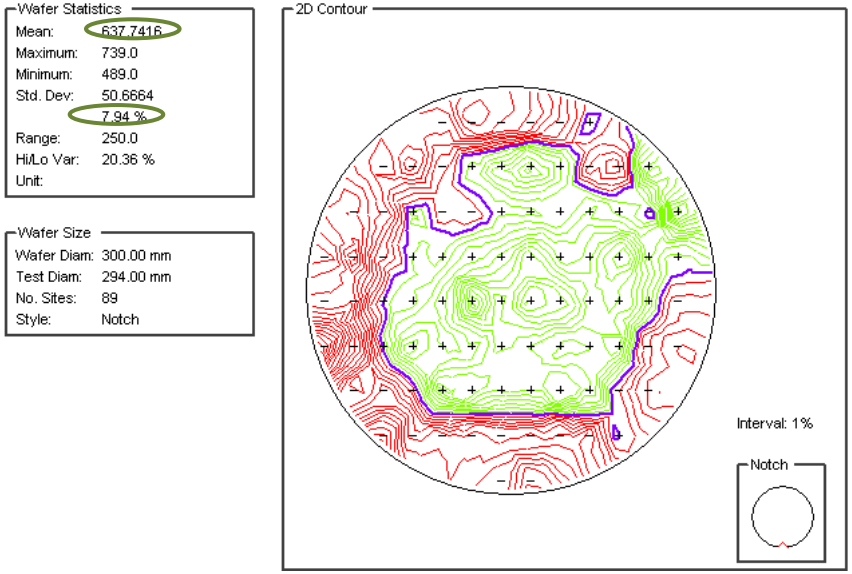


IBM 90nm cross section
D.Gill, et al., SPIE 2005

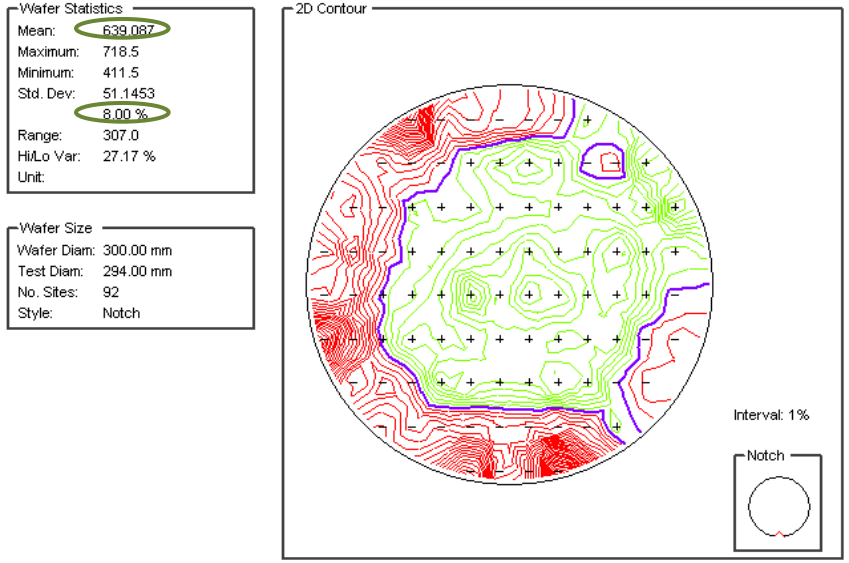
Probed vs. Non-Contact Measurements

45-nm SOI Wafer, Measured at Metal 2

Probed Measurements



Non-contact Measurements



Results Summary	Probed	Non-contact
Wafer Mean	637.7 MHz	639.1 MHz
Across Wafer Std. Deviation	7.94%	8.00%

- Non-contract results match probed results

Technology Summary

- Enables non-contact performance measurements of product-representative circuitry
  - Performance metrology augments physical metrology
  - Measurements are performed in-line as early as Metal 1, or as late as Metal Final
  - Small autonomous design enables both in-scribe and on-product placements
  - Standard CMOS designs built with standard process flow
- Non-contact results match probed results

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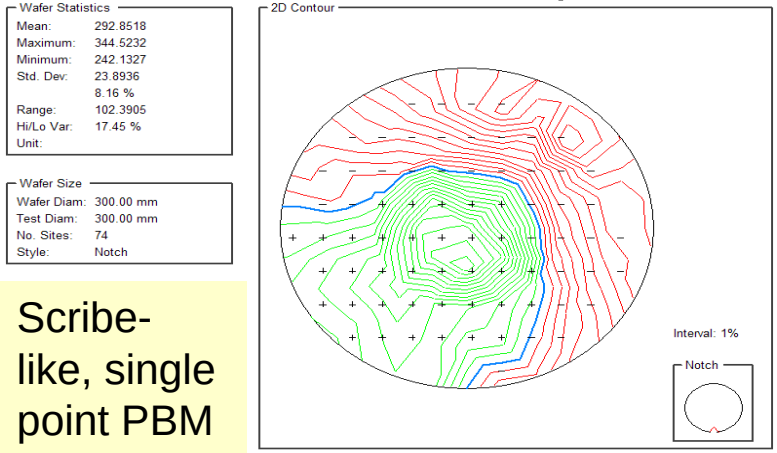
Cross-Wafer & Cross-die Variations

Scribe vs. Within-Die Measurements

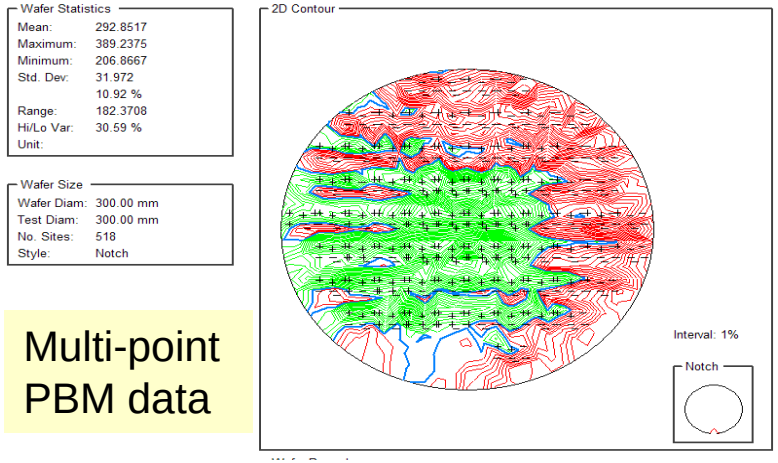
1 measurement site per field



Scribe-like, single point PBM data

17.5% Performance Variation in Scribe

8 measurement sites per field



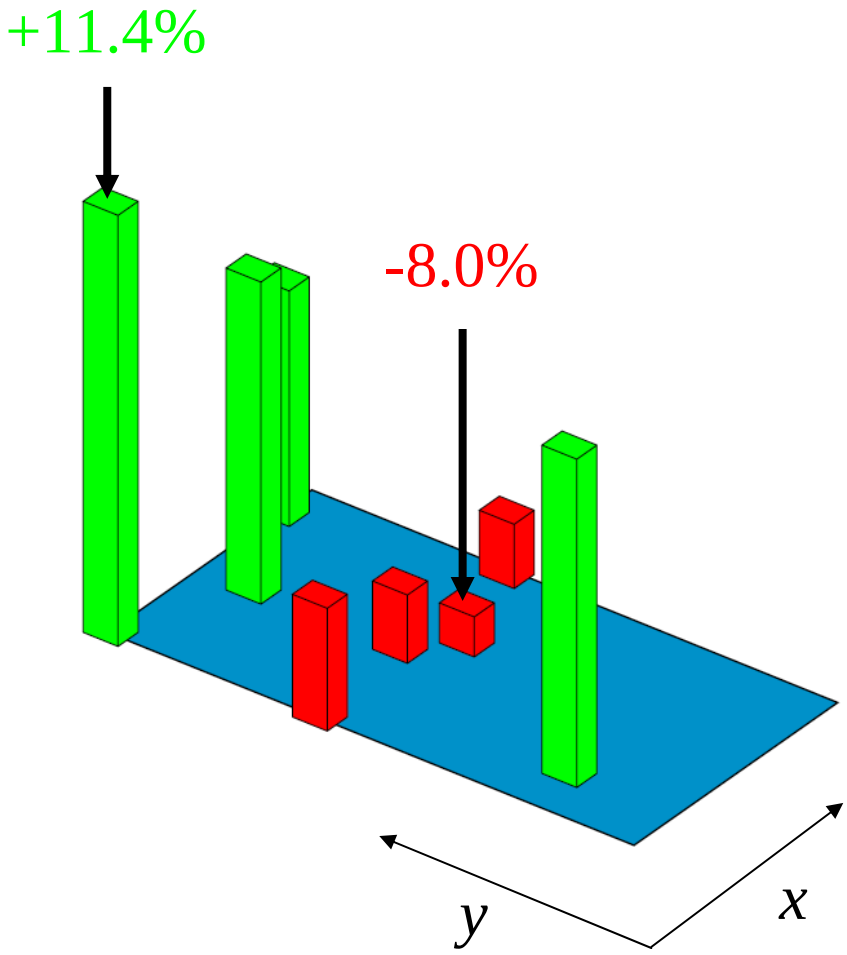
Multi-point PBM data

30.6% Performance Variation across Wafer

Scribe measurements do not capture the across-chip contributions to final-performance variation

Across-Die Variation

All Reticles Averaged



- Systematic in-die performance variation equals ~ 20%
  - Wafer edge is slower
  - Die edge is faster
- Scribe measurements do not capture in-die performance variation
- Cause of in-die variations is likely different than across-wafer variations

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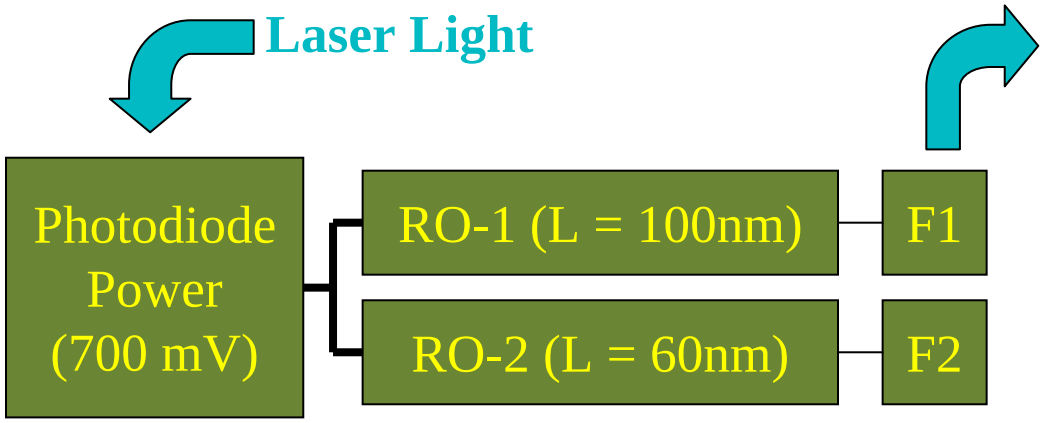
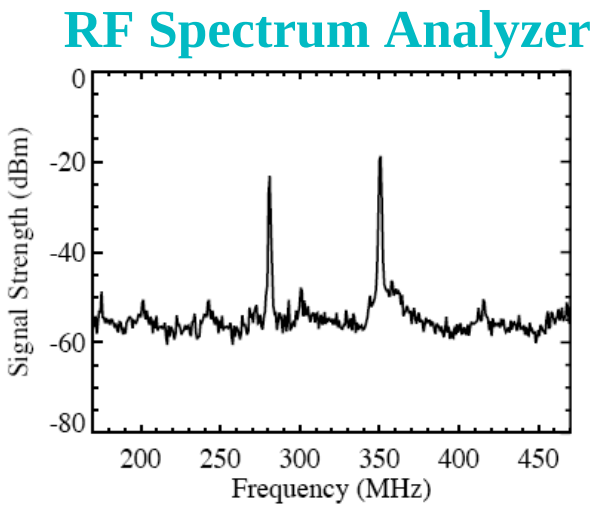
Differential Ring Oscillator Design for 65-nm Process

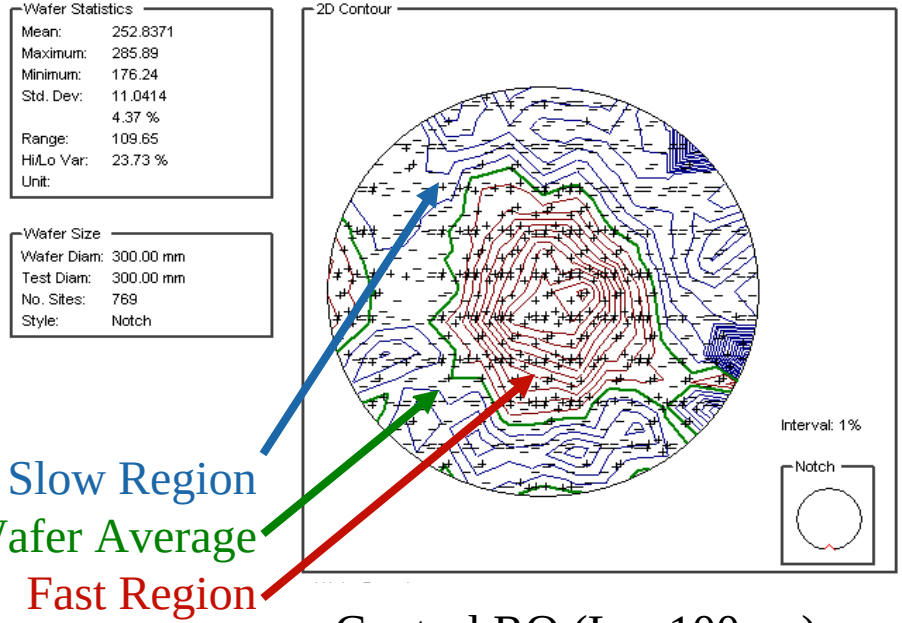
- One Photodiode powers two ROs in parallel
  - Control RO, long drawn gate length
  - Sensitive RO, nominal drawn gate length

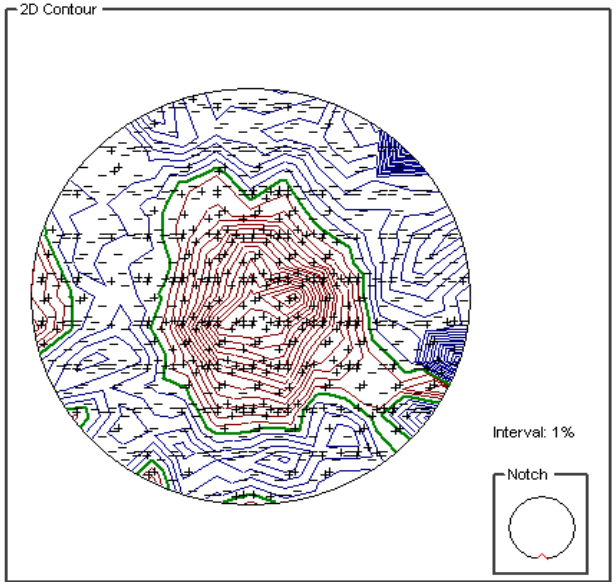




Across-Wafer Performance Data

Contoured wafermap presentation





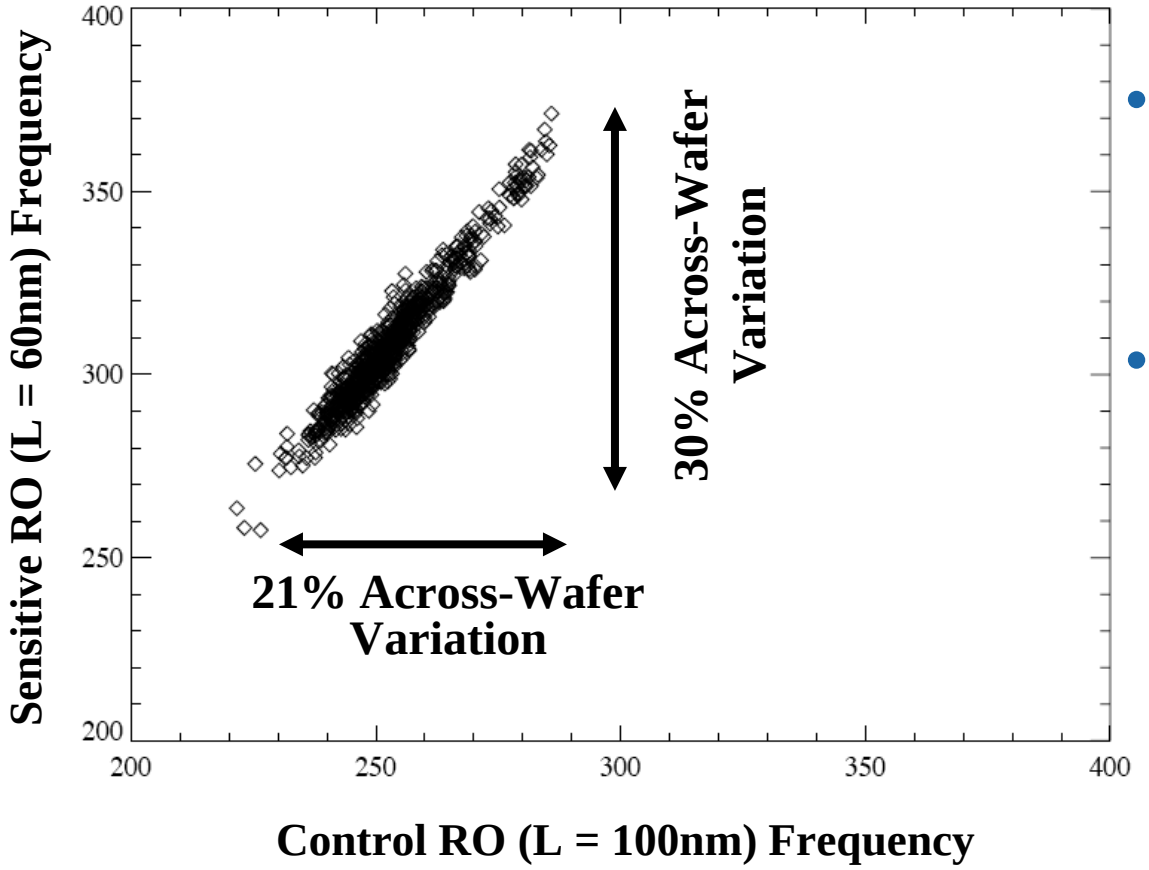
Control RO (L = 100nm)
Average Freq. = 252.8 MHz
1σ = 11.0 MHz

Sensitive RO (L = 60nm)
Average Freq. = 308.3 MHz
1σ = 18.1 MHz

770 Differential RO sites measured at M1

Across-Wafer Performance Data

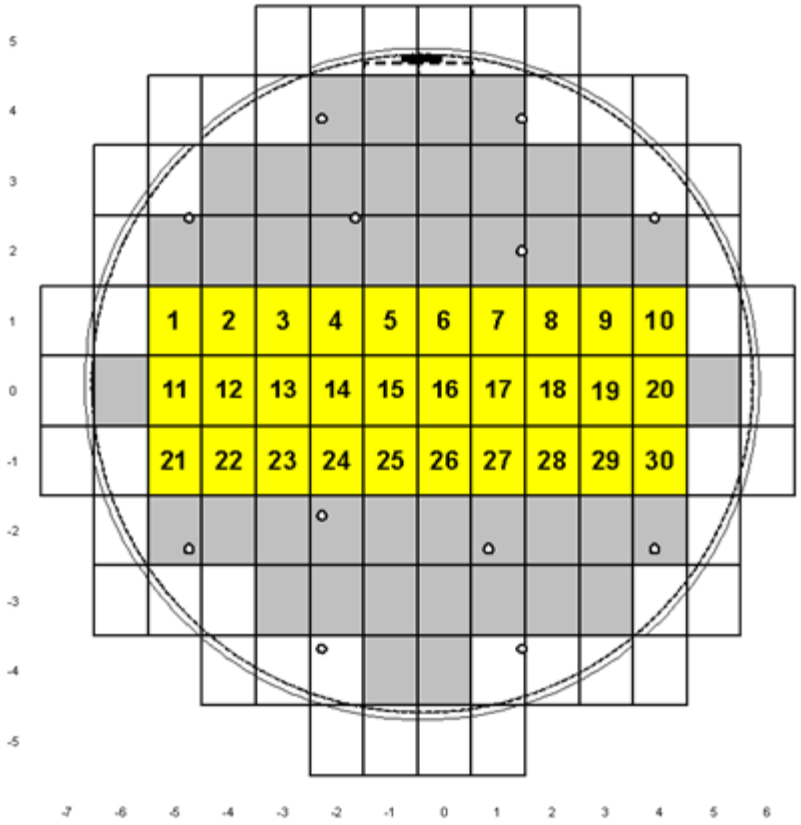
x-y scatterplot presentation, 770 data points



- Differential RO pairs correlate
- Larger across-wafer variation seen in short-channel "sensitive" RO

Wafer CD Poly Measurements

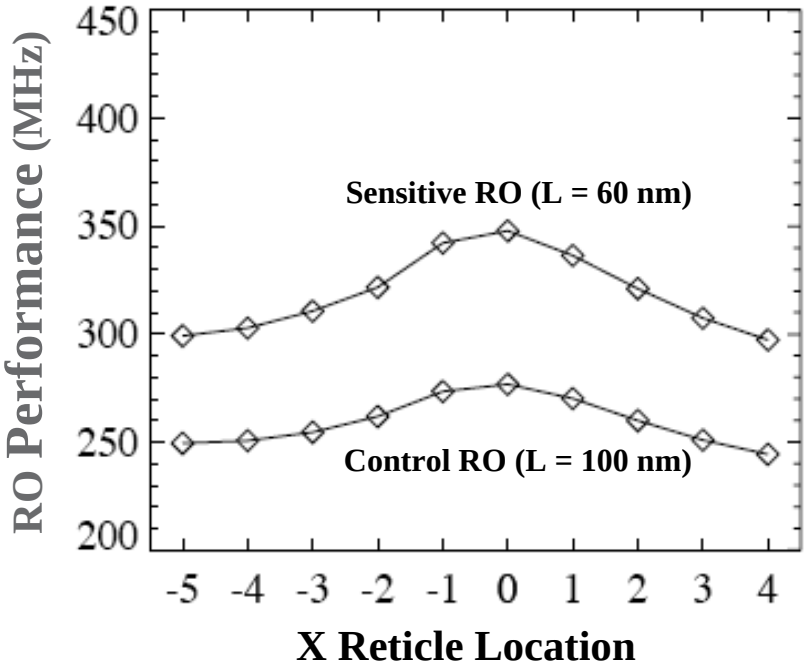
30 Sites, Target Production Poly = 64 nm

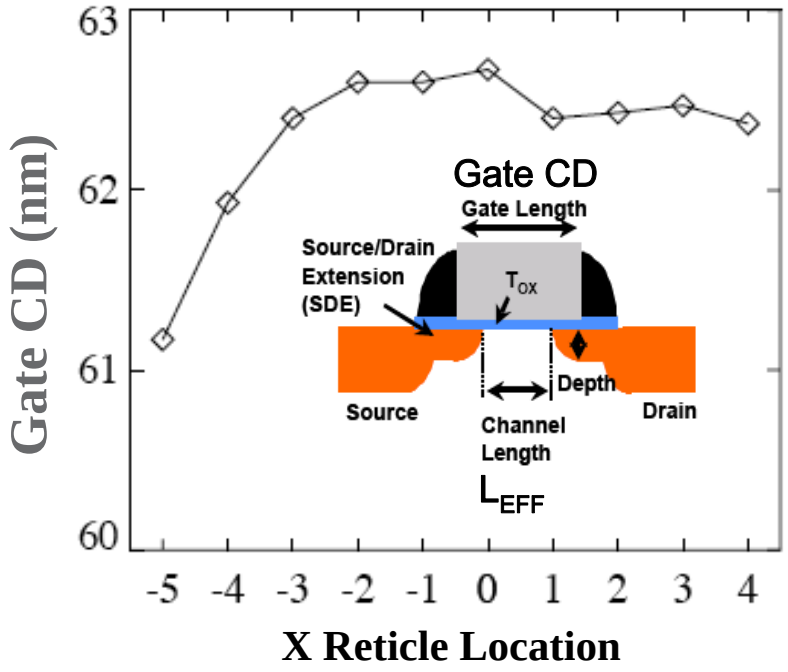


- Average CD = 62.3 nm
  - Min = 60.7 nm
  - Max= 62.9 nm
- 3.5% CD spread **cannot** explain 30% RO performance spread

Wafer Diameter Scan Comparisons

Measured RO Performance vs. Measured Gate CD

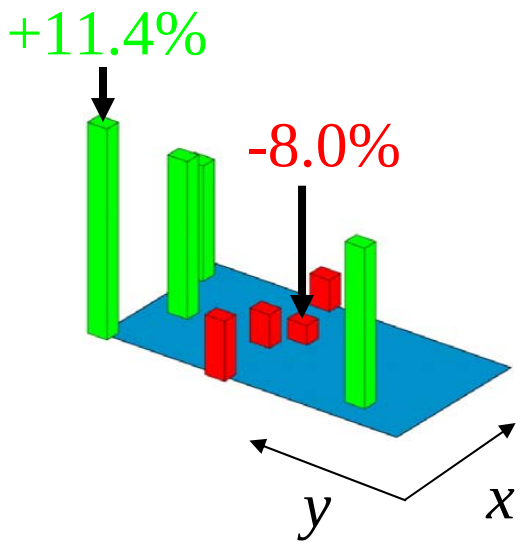




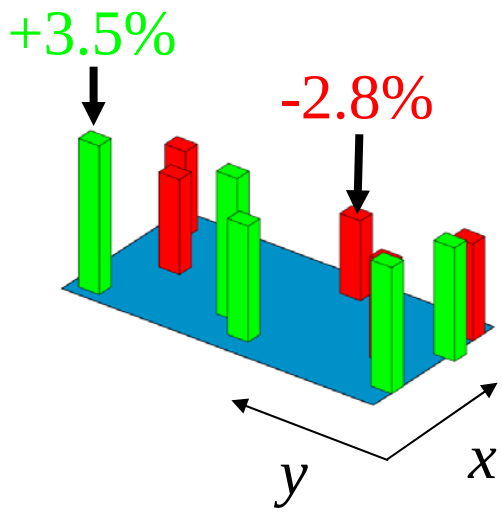
Measured performance (L_{EFF}) is <u>not</u> correlated with gate CD

Across-Die Variation

Sensitive RO (L = 60-nm), All Reticles Averaged



Early 65-nm process
(~20% in-die variation)

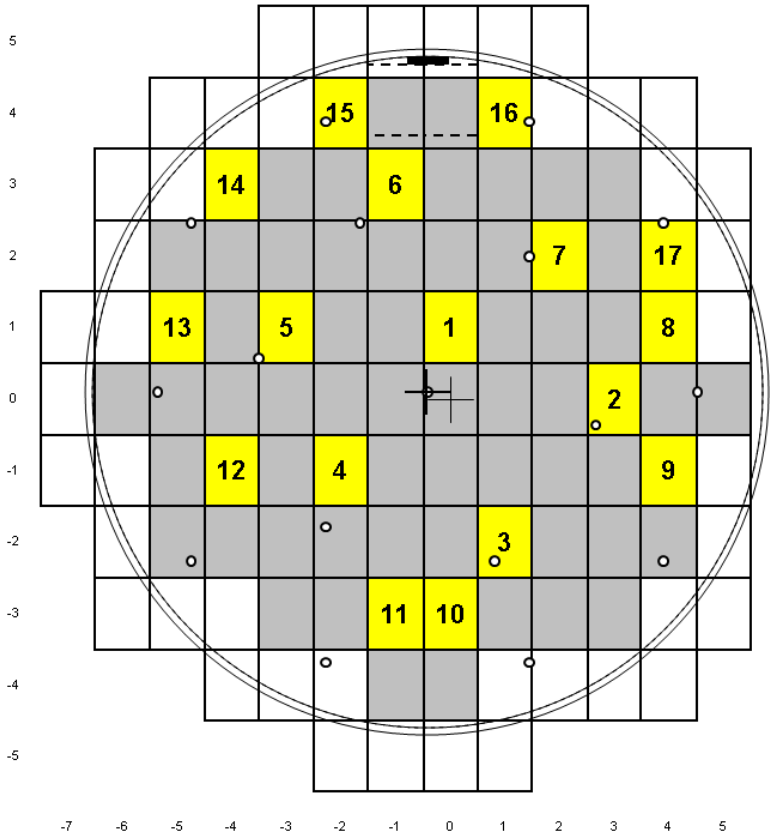


Improved 65-nm process
(~6% in-die variation)

- PBM Goal: Shorten yield ramp time using in-die performance characterization data

Etch-Trim Experiment

Target Production Poly Etch trim = - 4 nm



- Etch-trimmed CD
  - 58.7 nm average
  - Range = 58.0 to 59.0 nm
- Nominal wafer CD
  - 62.3 nm
- Change: -3.6 nm

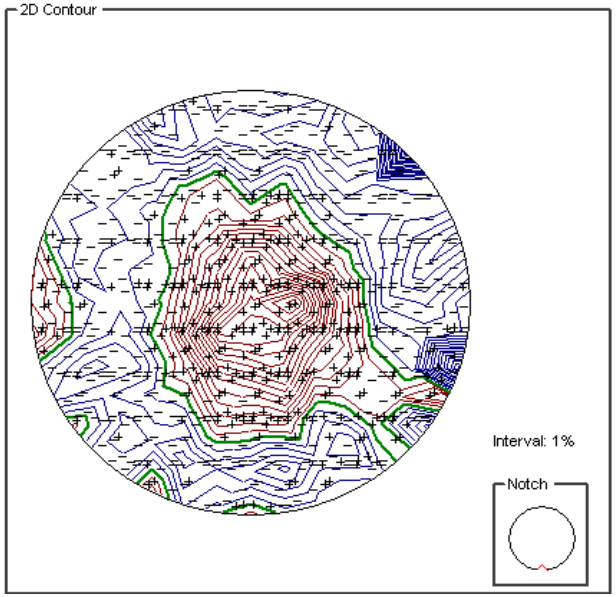
Note: 1.0 nm wafer CD uniformity!

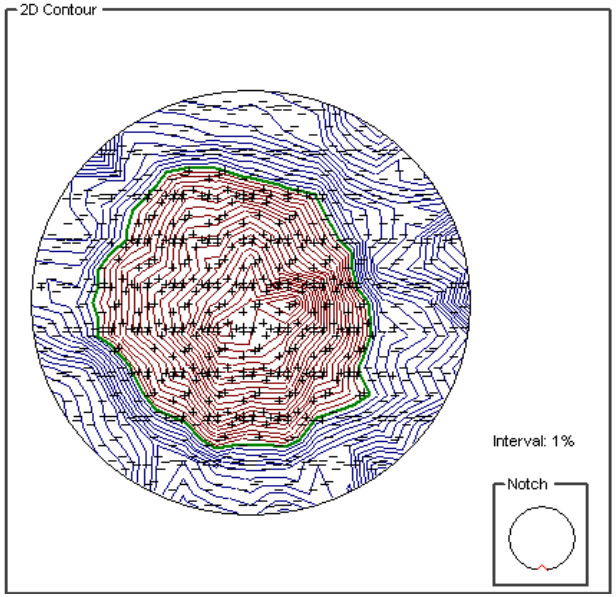
Across-Wafer Performance Data

Nominal Wafer vs. Poly Etch-Trim Wafer

Wafer Statistics	
Mean:	308.279
Maximum:	371.23
Minimum:	192.11
Std. Dev:	18.0712
	5.86 %
Range:	179.12
Hi/Lo Var:	31.80 %
Unit:	

Wafer Size	
Wafer Diam:	300.00 mm
Test Diam:	300.00 mm
No. Sites:	769
Style:	Notch





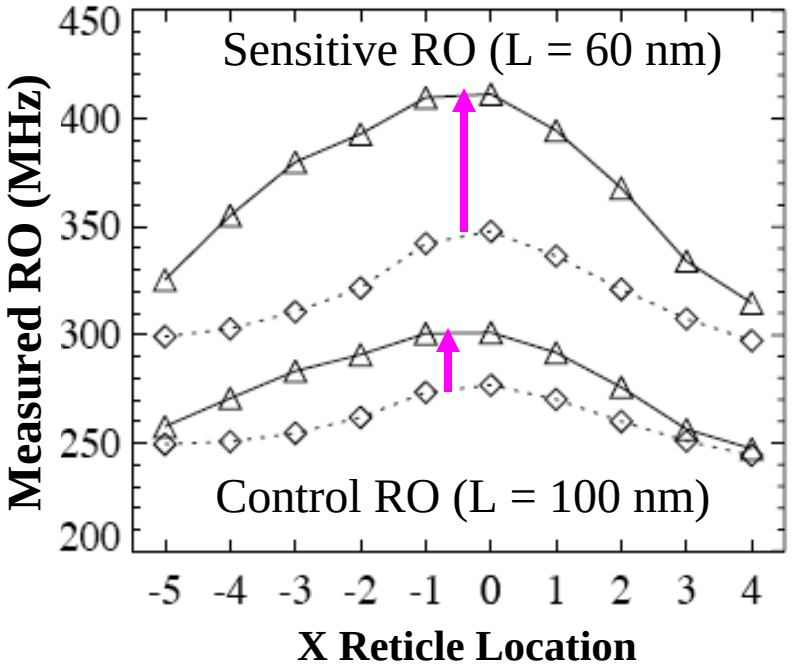
Nominal Wafer
Sensitive RO (L = 60nm)
Average Freq. = 308.3 MHz
1σ = 18.1 MHz

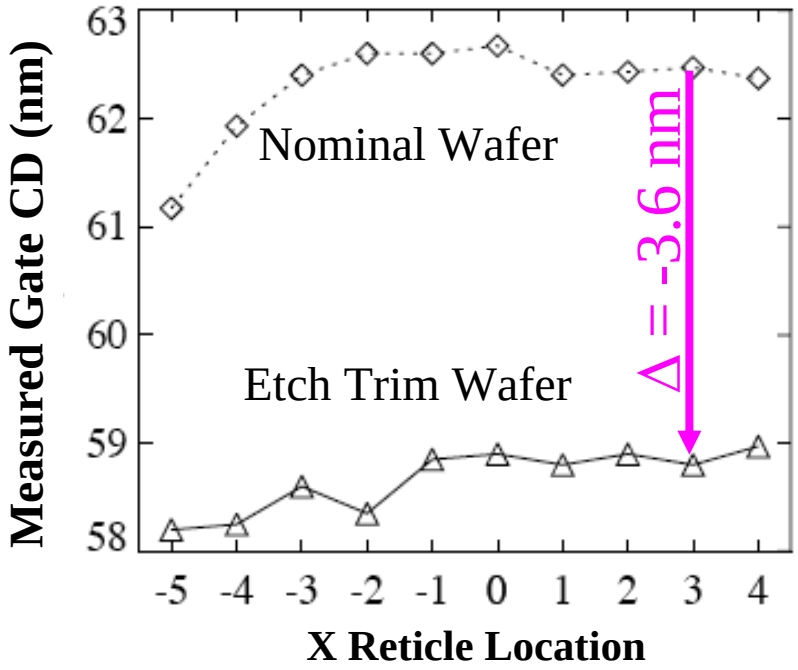
-4nm Poly Etch-Trim Wafer
Sensitive RO (L = 60nm)
Average Freq. = 338.8 MHz
1σ = 39.6 MHz

Speed increased < 10%, performance variation increased > 100%

Wafer Diameter Scan Comparisons

RO Performance vs. Gate CD

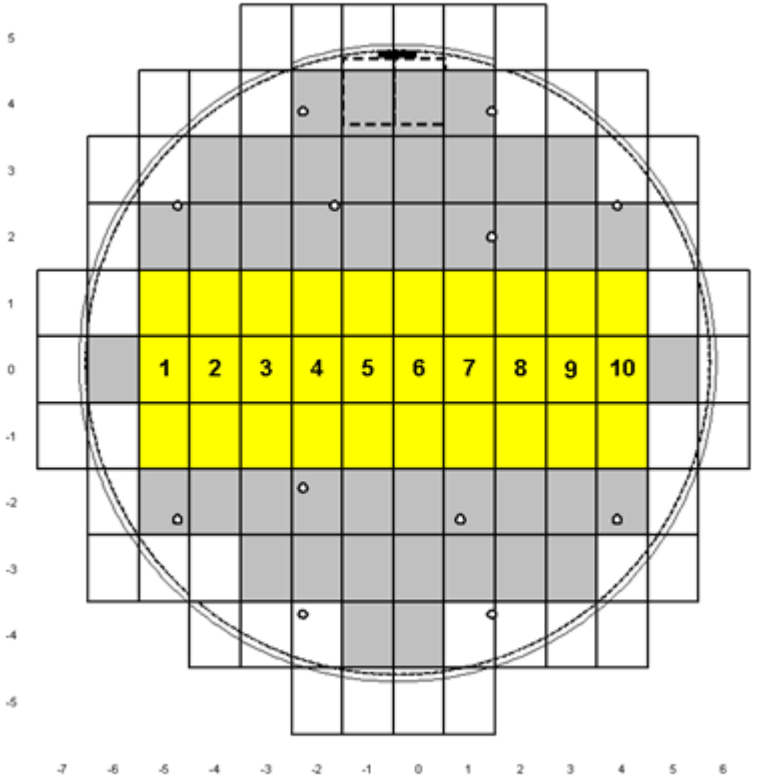


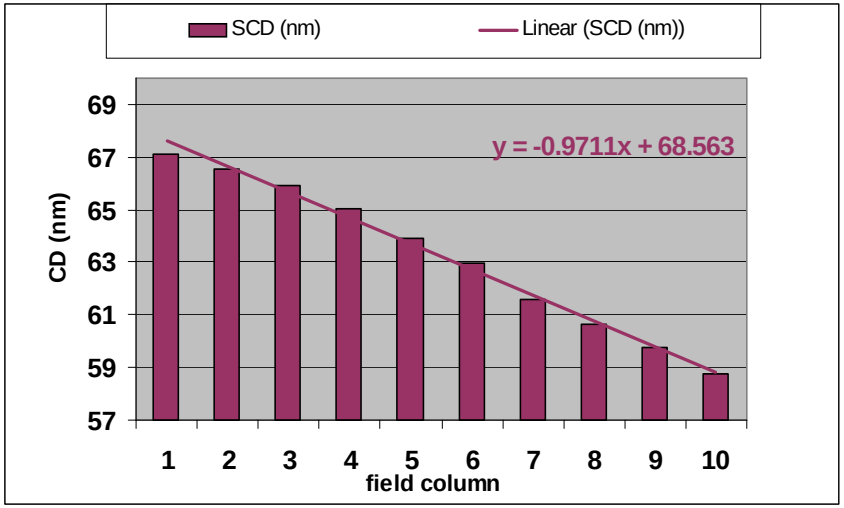


- Etch trim affects short-channel device more than long-channel device
- Measured performance (L_{EFF}) is <u>not</u> correlated with poly CD

Striped-Exposure Experiment

Target Poly CD Variation = -1 nm/stripe



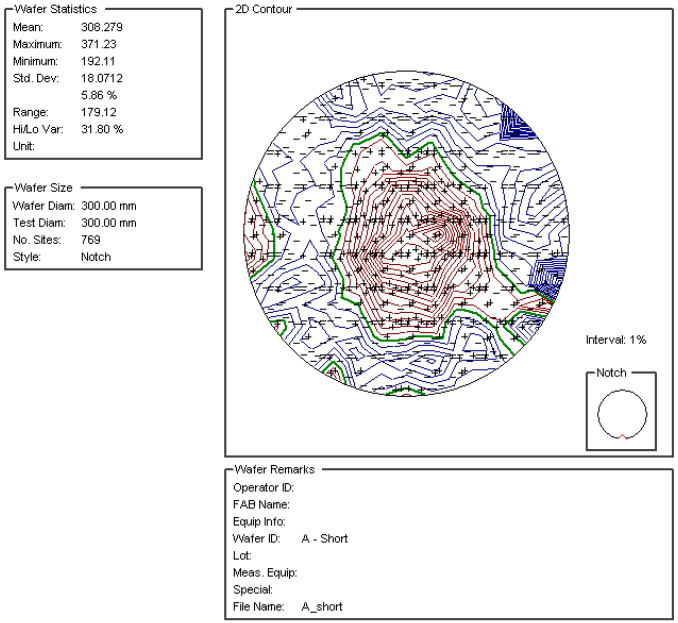


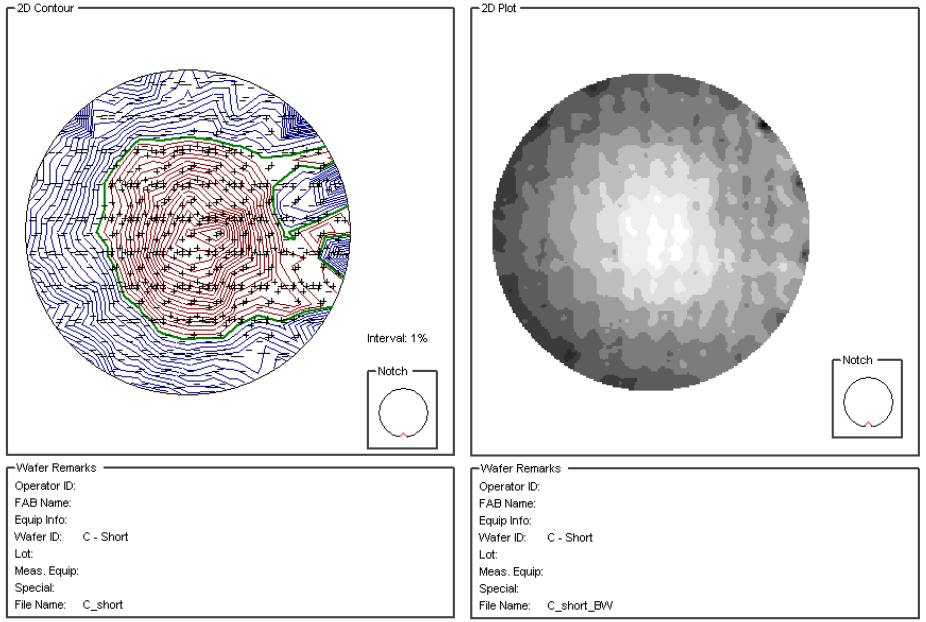
Measured poly CD changes
-0.97 nm / column

Column	1	2	3	4	5	6	7	8	9	10
SCD (nm)	67.1	66.5	65.9	65.0	63.9	62.9	61.6	60.6	59.8	58.8

Across-Wafer Performance Data

Nominal Wafer vs. Poly Striped-Exposure Wafer





Contour Representation

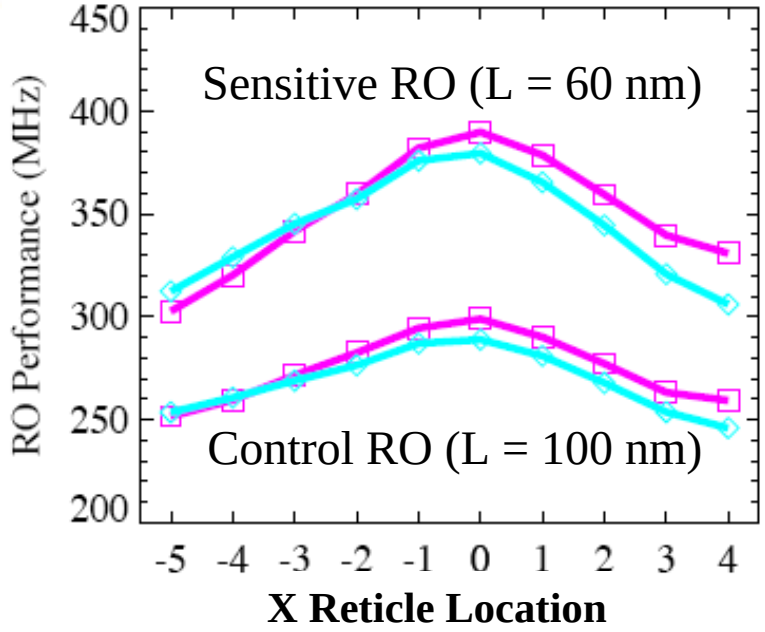
Greyscale Representation

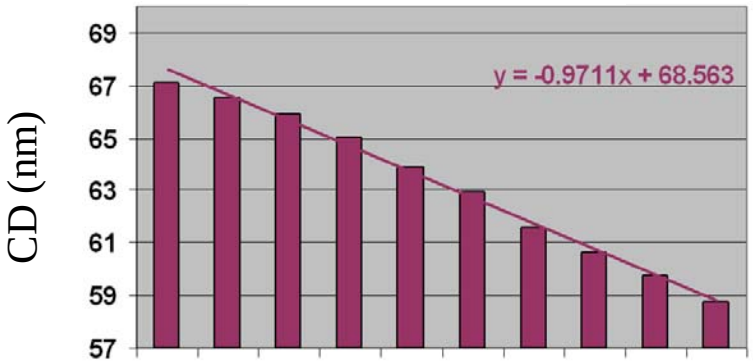
Nominal Wafer
Sensitive RO (L = 60nm)
Average Freq. = 308.3 MHz
1σ = 18.1 MHz

Poly Striped-Exposure Wafer
Sensitive RO (L = 60nm)
Average Freq. = 329.2 MHz
1σ = 32.1 MHz

Wafer Diameter Scan Comparisons

Nominal Wafer vs. Poly Striped Exposure Wafer





- Nominal Wafer
  - Measured poly CD uniform across wafer
- Striped Exposure Wafer
  - Measured poly CD varies from left to right
  - As poly CD shortens, RO performance increases
  - CD affect more pronounced on short-channel RO
- Across-wafer L_{EFF} variations still dominate exposure-induced CD variations

Experimental Summary

- Autonomous test circuitry and non-contact measurement capability enables routine in-line monitoring of across-wafer and in-die performance

- Poly gate CD does not correlate with performance
  - Small changes to gate length, as induced by etch trim and exposure splits, result in disproportionate variations to performance
  - Control of poly gate CD alone is not adequate for controlling product performance and final yield

"You can't control what you don't measure"

James S. Vickers - SEMICON Japan 2008

Performance-Based Metrology
Summary of Benefits

- Addresses the decreasing correlation between physical metrology and final product performance by enabling early measurements of product performance
- Addresses the decreasing correlation between scribe and in-die performance levels by enabling in-line, non-contact measurements of performance within the product itself
- Enables across-die, across-wafer, across-line, & across-fab monitoring and verification of the “contract” between the design and manufacturing groups
- Enables an accurate estimation of the final bin yield as early as M1