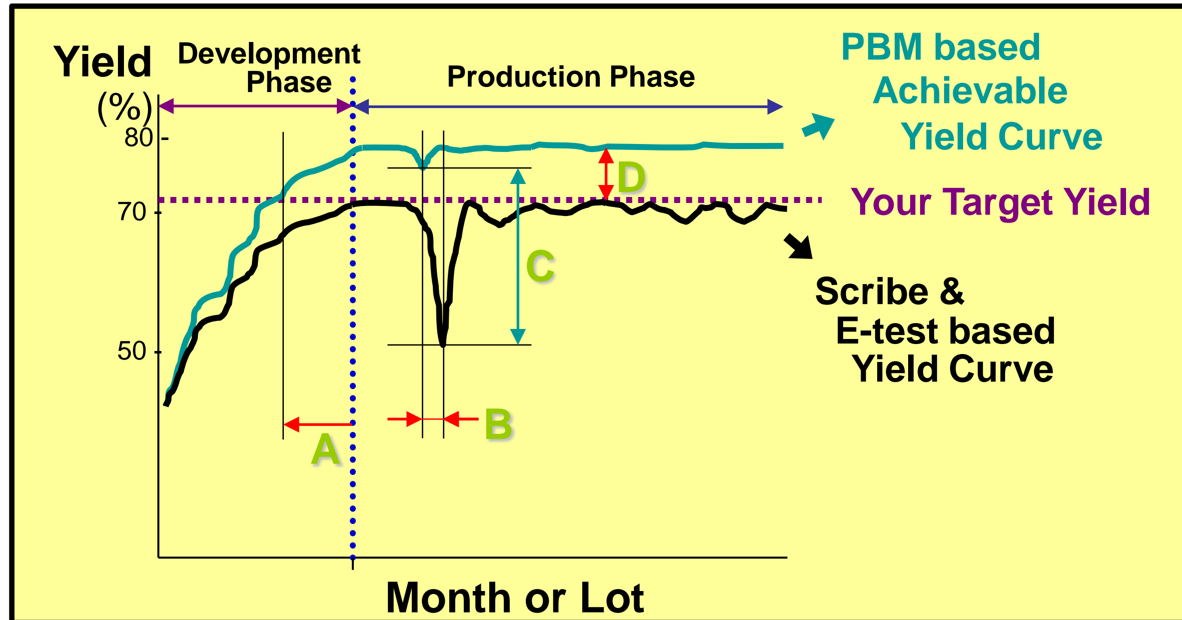
# tau-Metrix, Inc.

## A Product Yield Enhancement Company




- Enabling our customers to obtain and optimize:
  - **superior** indie product variability learning (early in the flow: metal 1)
  - **faster** product development ramp cycles
  - **enhanced** insight into design-process interactions
  - **improved** performance-based product yield



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# Value Statement

## Non-Contact, Pad-less Characterization Technology

- Industry Problem
  - **Increasing and dynamic offset** between scribe and in-die performance levels
  - **decreasing correlation** between physical metrology and final product performance
  - **costs** for special test-masks, off-line test, and lost product wafers
- The Solution: PBM Technology
  - small-footprint enables **pervasive in-die placements** (in-die variability)
  - autonomous design allows “drop-in” test structures, no wired power, no JTAG
  - enables **early, non-contact performance measurements** of product-representative ckts.
  - enables **continuous across-die, across-wafer, line-line, fab-fab monitoring,** and “contract” verification between design and manufacturing groups
  - **enhanced** process-design interaction **feedback** and improved forecasting of final bin yield
  - **faster product yield ramp** cycles and continuous process control
  - **early intervention** of process excursions to limit impact

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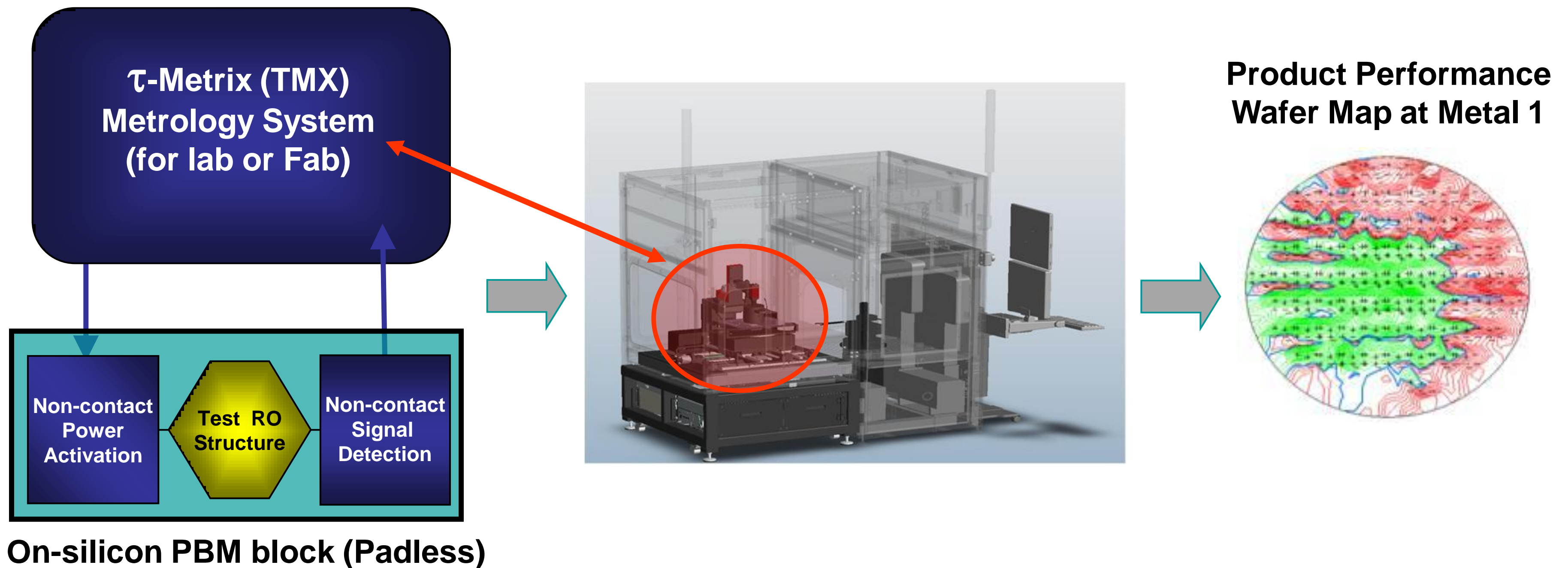
## A Product Yield Enhancement Company

- A pad-less, non-contact, performance-based metrology (PBM) technology
- The PBM technology: 1) measurement tool and 2) on-silicon test design
- Characterization of in-die and across wafer performance variability



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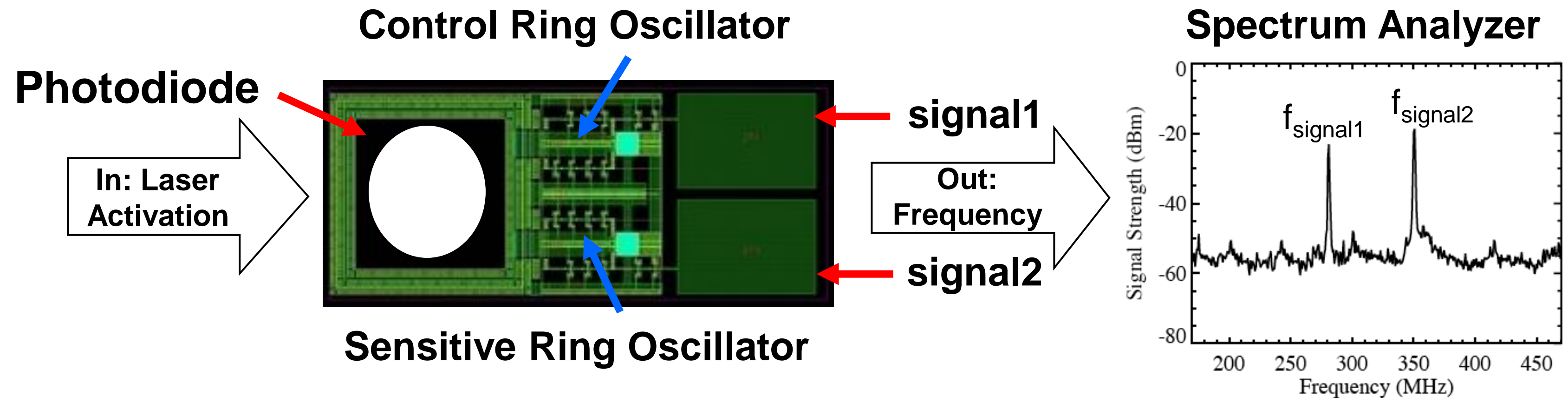
# On-Wafer PBM Structure

## Small Footprint, Pad-less, Autonomous design




- Small size: ~10 by 20 μm, can be placed in scribe or within product
- Pad-less, no-pin, electrically and functionally “autonomous” design
  - “Wire-less” activation powered and independent of surrounding circuitry
  - Uses standard CMOS design with user’s normal process flow
- Differential ROs (“control” and a “sensitive”) minimize the impact of:
  - Power supply variations common to both ROs
  - Typical ckts: INV, NAND, NOR, and customer-modified SRAM-based ROs



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# Standard Probe (contact) vs. PBM (non-contact):

*Direct one-to-one Comparison*

***45-nm SOI Inverter FO=1 RO Results at M2***

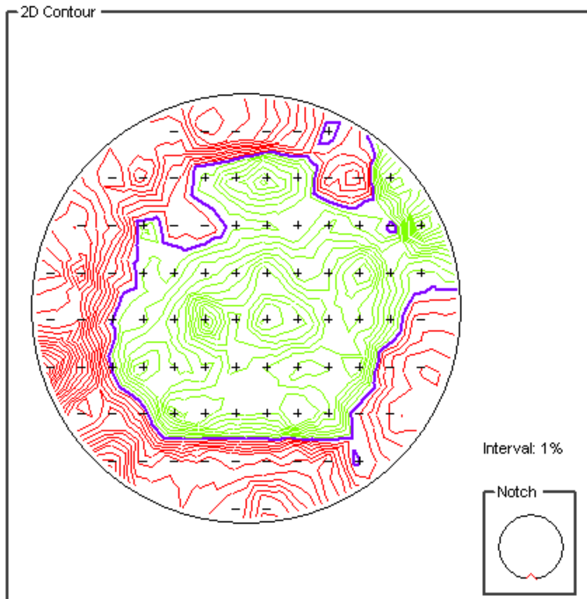
## Probed Measurements

**Wafer Statistics**

Mean: 637.7416
Maximum: 739.0
Minimum: 489.0
Std. Dev: 50.6664
7.94 %
Range: 250.0
Hi/Lo Var: 20.36 %
Unit:

**Wafer Size**

Wafer Diam: 300.00 mm
Test Diam: 294.00 mm
No. Sites: 89
Style: Notch



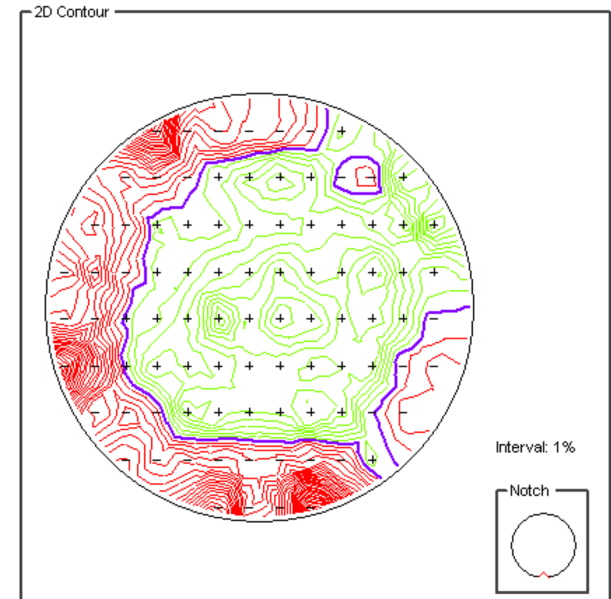

## TMX Non-contact Measurements

**Wafer Statistics**

Mean: 639.087
Maximum: 718.5
Minimum: 411.5
Std. Dev: 51.1453
8.00 %
Range: 307.0
Hi/Lo Var: 27.17 %
Unit:

**Wafer Size**

Wafer Diam: 300.00 mm
Test Diam: 294.00 mm
No. Sites: 92
Style: Notch




| Results Summary | Probed | Non-contact |
|---|---|---|
| Wafer Mean | **637.7 MHz** | **639.1 MHz** |
| Across Wafer Std. Deviation | **7.94%** | **8.00%** |

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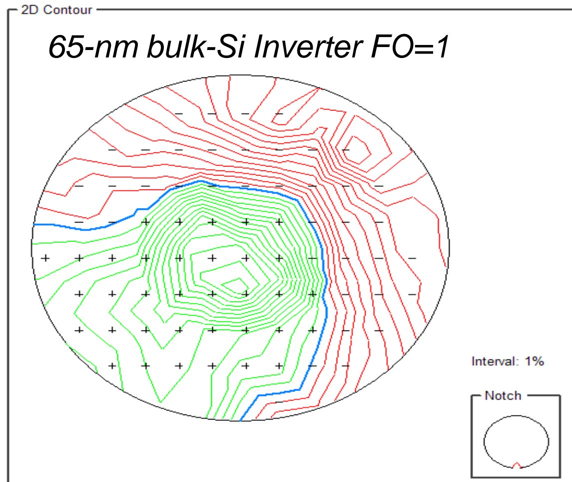
# Multi-Point In-Die PBM Benefit:

*Early, fast, non-destructive/contact, performance measurements to Assess Local (in-die) and Global (wafer-level) Performance Variation*

## 1 measurement site per field

Wafer Statistics
Mean: 292.8518
Maximum: 344.5232
Minimum: 242.1327
Std. Dev: 23.8936
8.16 %
Range: 102.3905
Hi/Lo Var: 17.45 %
Unit:

Wafer Size
Wafer Diam: 300.00 mm
Test Diam: 300.00 mm
No. Sites: 74
Style: Notch



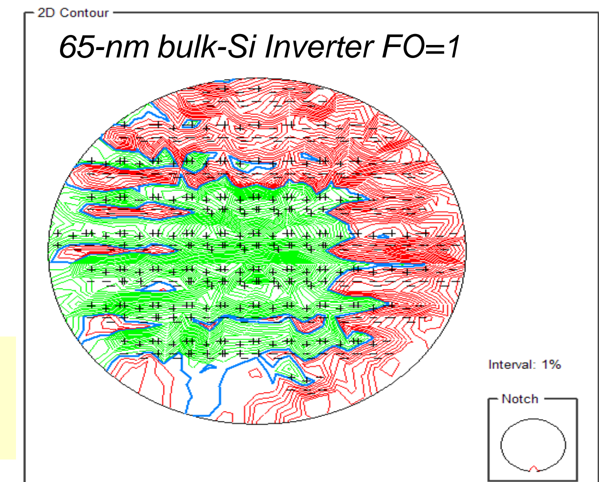

Scribe-like, single point PBM data

Drawn Gate: 60 nm
292 MHz 17.5%

## 8 measurement sites per field

Wafer Statistics
Mean: 292.8517
Maximum: 389.2375
Minimum: 206.8667
Std. Dev: 31.972
10.92 %
Range: 182.3708
Hi/Lo Var: 30.59 %
Unit:

Wafer Size
Wafer Diam: 300.00 mm
Test Diam: 300.00 mm
No. Sites: 518
Style: Notch




Multi-point PBM data

Drawn Gate: 60 nm
292 MHz **30.6%**

- **Single point/scribe measurements and physical metrology do not sufficiently capture across chip variation (ACV) contribution to in-die performance variation**
- **Key in-die process sensitivities are missed with conventional scribe measurements**



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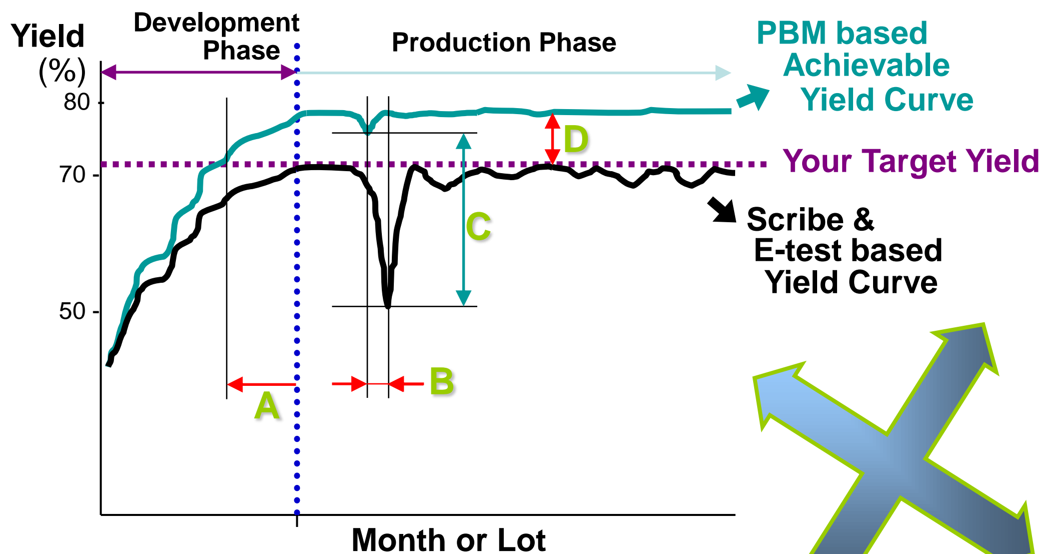
# Performance-Based Metrology (PBM)
## Applications

- Early Technology Development Phase:
  - Quick-cycle device/process characterization
  - Process ($V_t$, $L_{poly}$, Rx, anneal) sensitivity learning
  - Health-of-line, ACLV, Local and Global tracking assessment
  - Improved feedback for design rules and models (ACV, etc.)
- Product Ramp and Production Phase:
  - Improved ROI
  - Quicker Design-Process interaction feedback
  - Accelerated product-yield ramp
  - Continuous monitoring of in-die performance metrics

# PBM Yield Improvement

## Time-Dependent (Product Dev./Ramp) and Final




**Effect B & C :**

**tau-Metrix PBM technology provides process variation monitoring in timely manner. Deep yield-loss excursions will be minimized with very short TAT, which obviates the wait time (delay) for E-test results.**

**Cost Savings !!!**

**Effect A :**

**tau-Metrix PBM technology provides performance-based measurement data at M1. It helps to manage both process variation and yield. It is also an enabler to achieve product yield targets earlier than the conventional schemes, which minimizes lead time.**

**Time to Market !!!**

**Effect D :**

**tau-Metrix PBM technology collects in-die process variation data at M1. It can monitor and improve process continuously, which can accelerate production cycle times. The early and enhanced learning can improve and maintain higher final yield levels.**

**Increase Revenue !!!**

# ROI

## MPU Example (Yield Improvement + Bin Allocation Shift)

| Fab Balance Sheet, per Month | | |
|---|---|---|
| Wafer Production Costs | Standard Metrology | Performance-Based Metrology |
| @ M1 | $1,500.00 | $1,500.00 |
| @ MF | $2,500.00 | $2,500.00 |
| Wafer Starts | 30000 | 30000 |
| Wafers Pulled @ M1 for Test | 300 | 30 |
| Reticles per Wafer | 74 | 74 |
| Die per Reticle | 4 | 4 |
| Failing Product | 30% | 25% |
| Bin 2 Product Yield | 50% | 40% |
| Bin 1 Product Yield (best perf.) | 20% | 35% |
| Good Die Produced | 6,153,840 | 6,653,340 |
| Fab Costs ($M) | $74.7 | $75.0 |
| Cost per Good Die | $12.14 | $11.27 |
| Manufacturing Savings | --------------> | -7.17% |
| Bin 2 Product Value | $80.00 | $80.00 |
| Bin 1 Product Value (best perf.) | $140.00 | $140.00 |
| Product Revenue ($M) | $597.8 | $718.6 |
| Gross Profit ($M) | $523.1 | $643.6 |
| Increased Monthly Profit ($M) | --------------> | $120.5 |

Note: Improvement in product-yield ramp (in time) is not incorporated in this analysis

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- Extended: Background Information
- Supporting Measurements and Analysis



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# Increasing and Dynamic Offset

*Scribe to in-die correlation is a weak link*

IBM Research - Austin

## An Opportunity Exploited... IBM/MIT

- Current state of the art in variability characterization:
  - Single transistors in scribe lanes from which BSIM parameters are (laboriously) extracted.
  - Process-control-oriented physical test structures to estimate/track physical parameters (e.g. $\Delta L$).
- Problems:
  - Test structures **do not look like real circuits** and so miss the layout-dependence of variability in the sub-wavelength regime.
  - Spatial resolution low so within-die variability can only be roughly estimated.
  - Characterization is labor intensive so gets done very infrequently.

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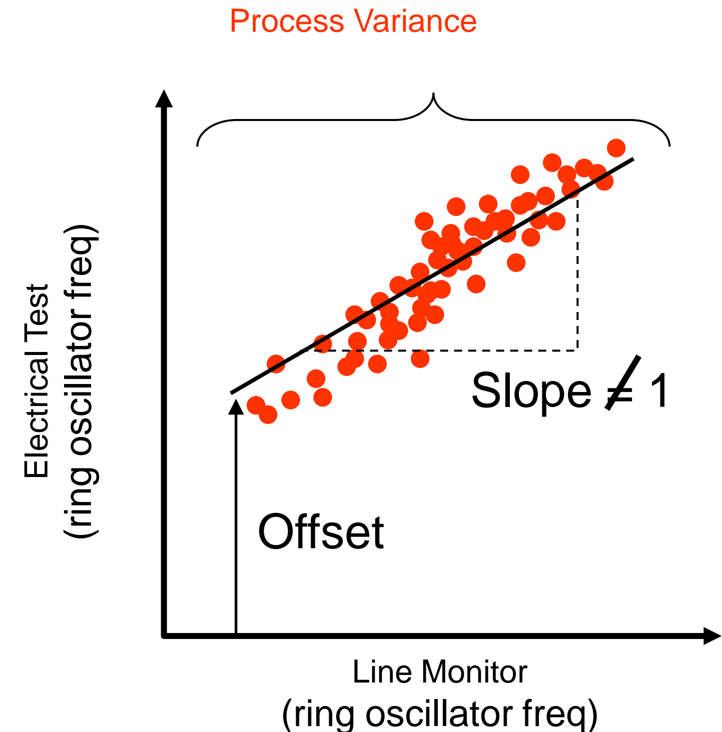


*"Challenges in the Design Manufacturing Interface" S. Nassif, IBM, ICCAD 10/03*

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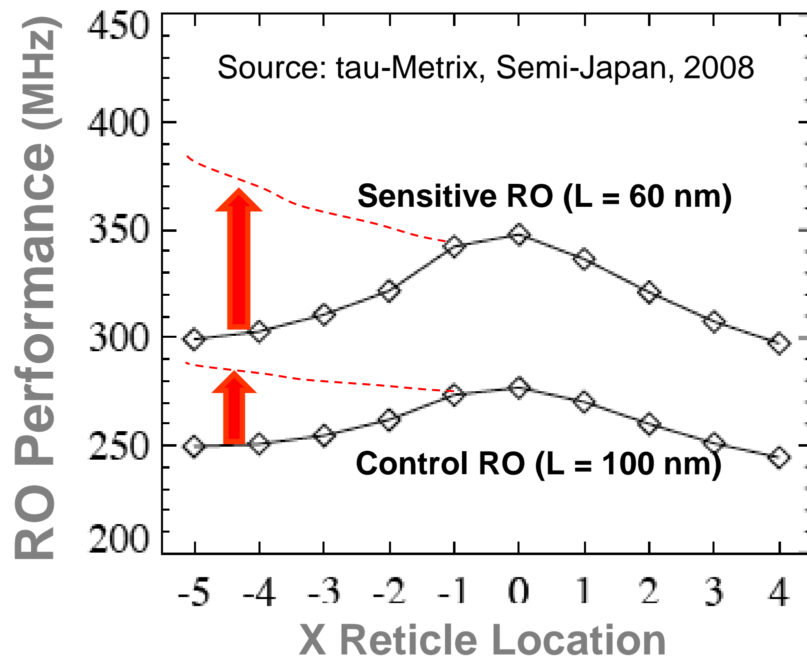
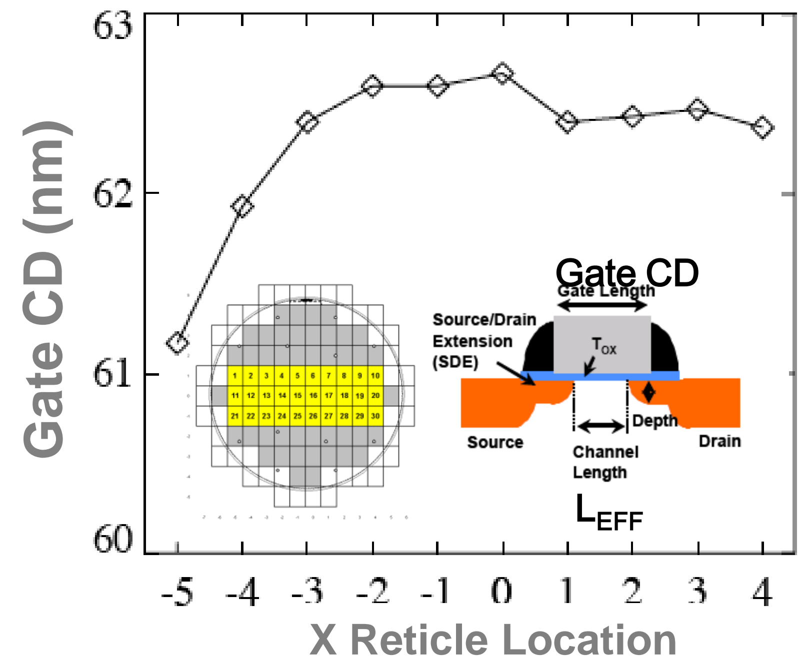
# Decreasing Correlation

*Physical Metrology vs. final product performance*




- Wafer CD Poly Measurements - Target Poly = 64 nm
- 3.5% CD spread **cannot** explain 30% RO performance spread
- Measured RO performance ($L_{EFF}$) is not correlated with gate CD

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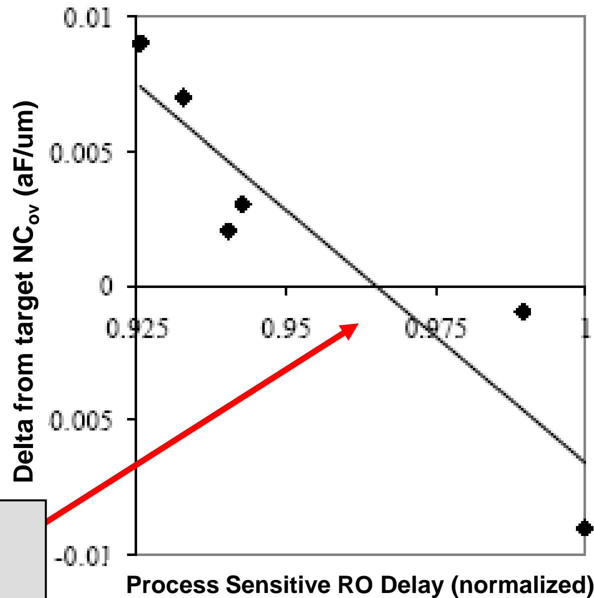
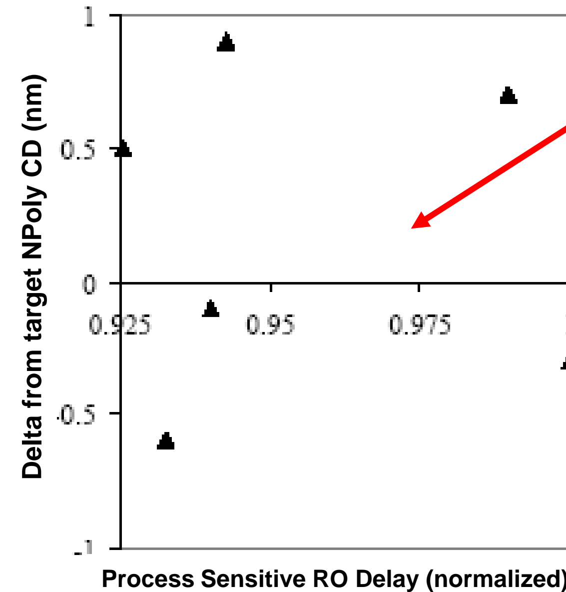
# Decreasing Correlation

*≤ 90nm the physical CD control ≠ expected final performance*




No correlation of CD to RO delay

Overlap Capacitance ($C_{ov}$) main driver of $L_{eff}$ variation

- Physical Gate Length and $C_{ov}$ together determine $L_{eff}$.
- Physical metrology cannot measure $C_{ov}$.

Source: A. H. Gabor et al, IBM, 2007 SPIE Microlithography

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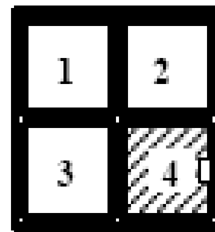
# Decreasing Correlation of Physical Metrology

## "Bad" wafers look "good" to dimensional metrology inspections

### Typical scenario

- In-line metrology is good (1%-2% 3σ uniformity for processes)
- But Yield is low near wafer edges
- Cause: final test studies reveal excessive in-chip performance variation (as high as 15%)

*M. Orshansky, C. Hu (UC Berkeley)*



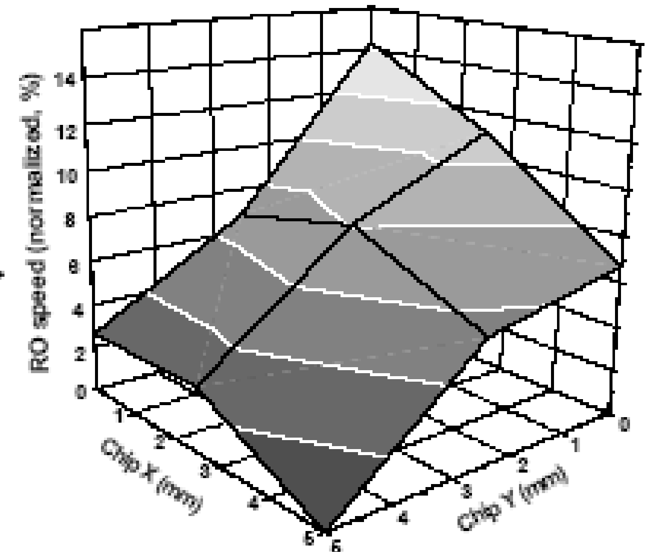




**Figure 4.** As a result of spatial Lgate variability, the circuit timing properties significantly vary across the chip. (Chip 4 is shown).

**Dimensional metrology inspections can miss in-chip performance variation**

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# PBM Applications (Detailed)

*Time-to-market: Technology Development and Productization Phases*

- **Process:** Direct measurement (non-filtered and averaged with larger number of gates averaging– and/or frequency-counters), and fast (w/ first-connectivity vs. end-of-line) performance impact of design, lay-out and process (e.g. $V_t$, $L_{poly}$, Rx, anneal)
- **Design/Integration:** Sensitivity and marginality learning and optimization
- **Quick-cycle to final-performance** data (immediately with first-connectivity, ≥ M1) device/process characterization
- Strong PBM “differential” signature and sensitivity enables recognizing immediately +/- **gate-CD variations**
- **Improved feedback** for design rules and device models (ACV, etc.)



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# PBM Applications (Detailed)

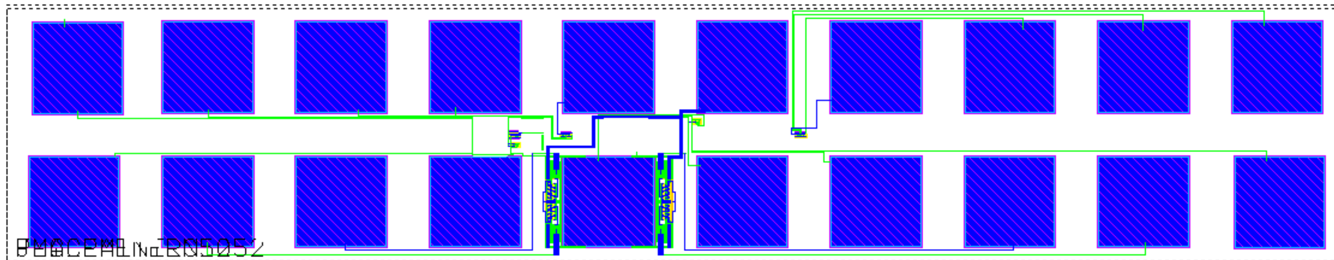
## *Product Ramp and Production Phase*

- **Improved ROI** (e.g. estimated MPU bin-sort improvement: > 20%) by immediate and early correlation and subsequent process and design improvement for bin/sort (performance) yield
- **Accelerated information feedback loop** for product development and yield ramp
  - Typically in-line measurement 600 sites/hour at M1
  - Hour per wafer (for 600 measurements) versus additional 6-12 weeks from M1 to MF.
  - Non-contact measurements require no post-measurement cleaning. Wafers will be re-introduced into the process.
- **Design, process and integration:**
  - "Quicker (weeks versus months) Design-Process interaction feedback
  - Higher sensitivity than physical CD (e.g. 20% PBM vs. 5% gate CD variation on 65nm)
  - Health-of-line",
  - Electrical and physical device parameters (Vt, $L_{poly}$ … )
  - ACLV, Local (e.g. field) and Global (fab) tracking assessment
  - Continuous (in-line) monitoring and base-lining (of critical modular metrology) of in-die (active product) composite (versus discrete physical processes) final performance metrics
  - Integration: Die-to-die, wafer-to-wafer, lot-to-lot, line-to-line, fab-to-fab early and standard base-line and comparisons

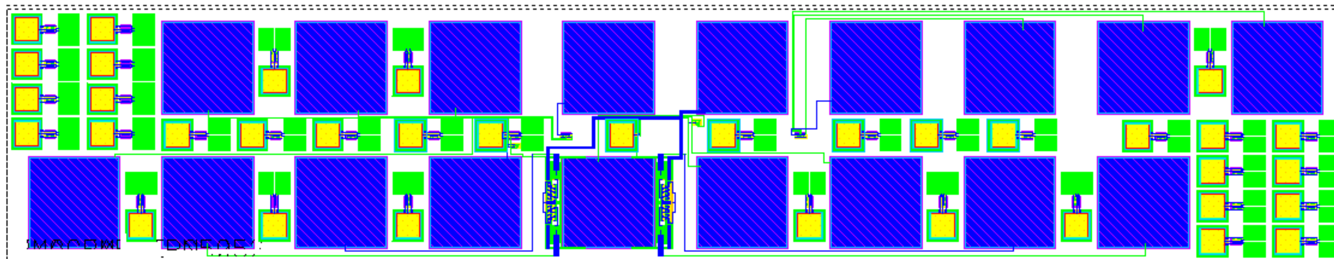
# Illustration of Small Footprint Benefits

*Small Footprint, autonomous, drawn directly from product (65nm Example)*

- ORIGINAL: two RO, PFET & NFET(counters, control logic, and pad buffers)



- PBM + ORIGINAL: two RO, PFET & NFET(counters, control logic, and pad buffers)



- PBM + ORIGINAL: Included original two ROs + 33 additional PBM process and device characterization structures for supplementary learning
- PBM only (no pads): Potential for > 125 PBM test structures within same space



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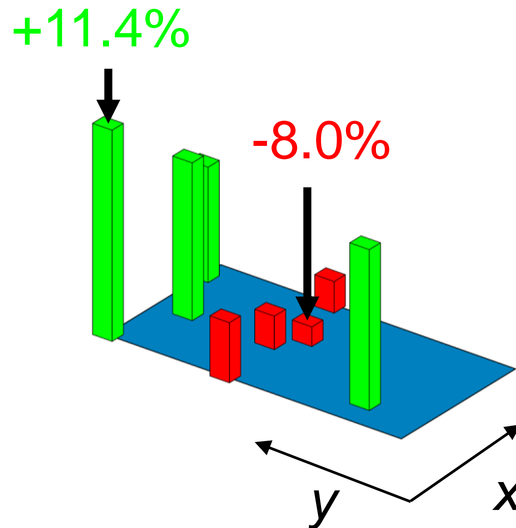
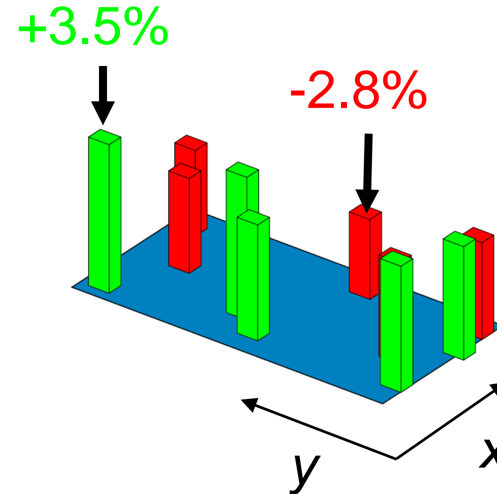
# Potential for Faster Yield Ramp

*65nm bulk-Si, Sensitive RO (L = 60-nm), All Reticles Averaged*




Early 65-nm process
(~20% in-die variation)




Improved 65-nm process
(~6% in-die variation)

- Across-Die Variation Improvement Observed
- Shorten yield ramp time using in-die performance data

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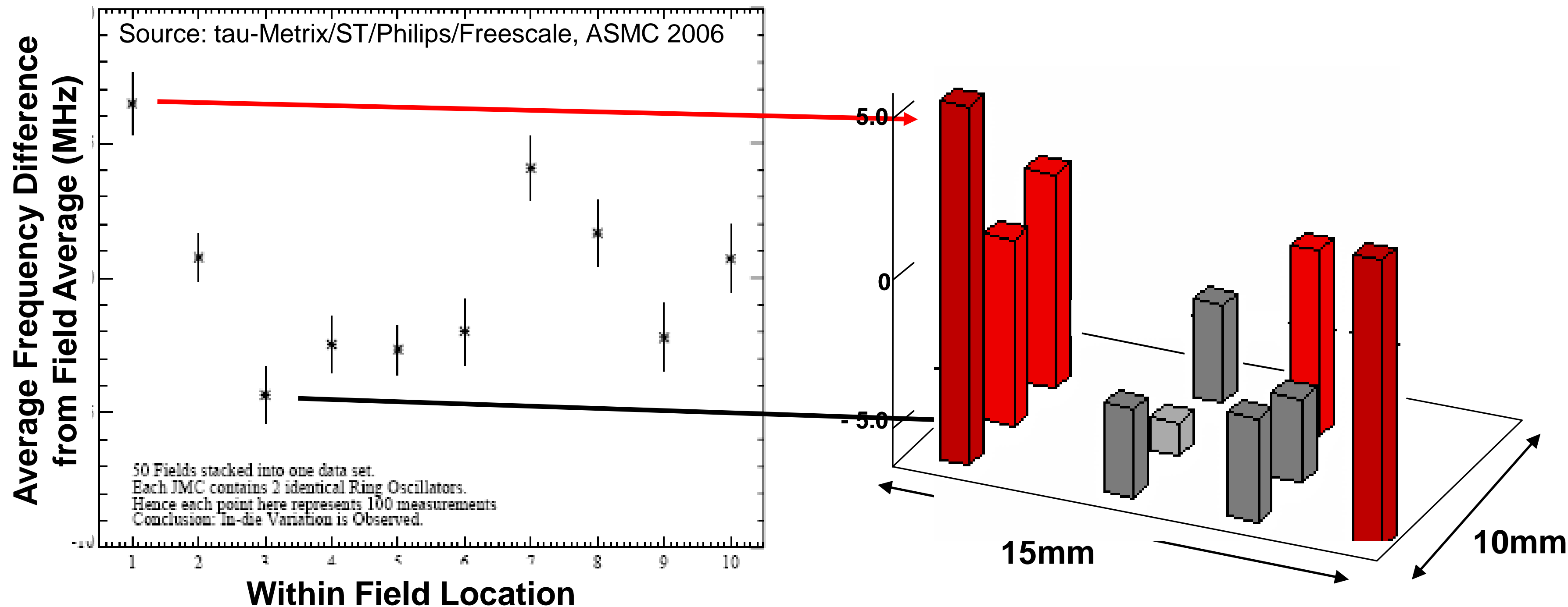
# Captures Key In-Die Process Sensitivities

*Non-contact PBM measurements of in-chip Ring Oscillators, 90nm Process*




- **Key in-die process sensitivities are missed with conventional single-point scribe measurements**



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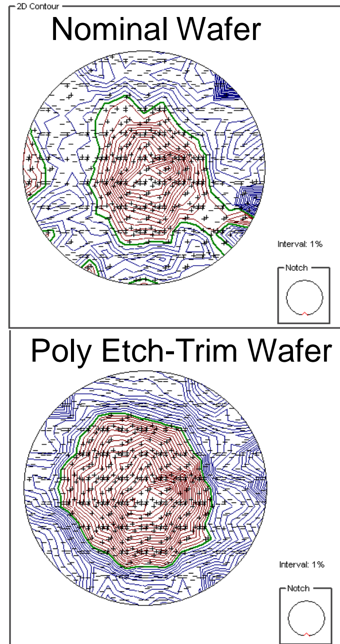
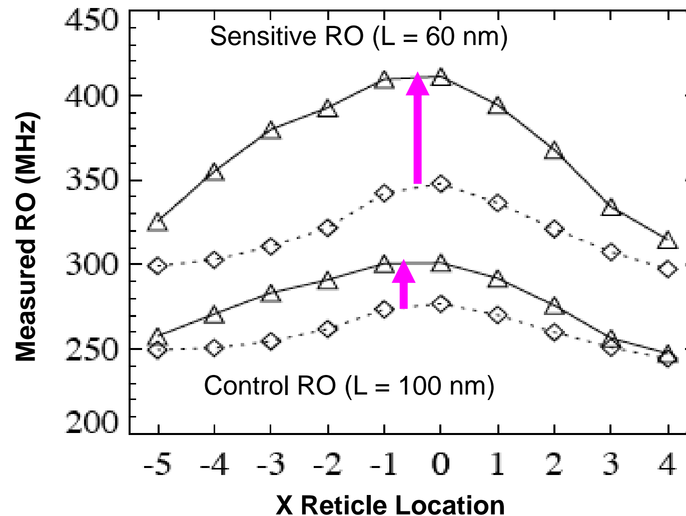
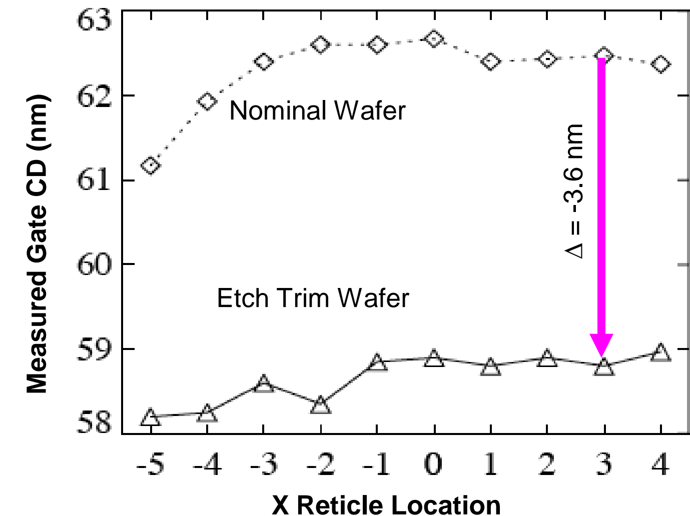
# Decreasing Correlation (continued)

## Gate Poly Etch-Trim *RO Performance Sensitivity: PBM » Physical CD*




- Nominal Wafer, RO (L = 60nm), Ave. Freq.= 308.3 MHz, 1s =18.1 MHz
- -4nm Poly Etch-Trim Wafer, RO (L = 60nm), Ave Freq. = 338.8 MHz, 1s= 39.6 MHz
- Speed increased < 10%, performance variation increased > 100%
- Etch trim affects short-channel device more than long-channel device



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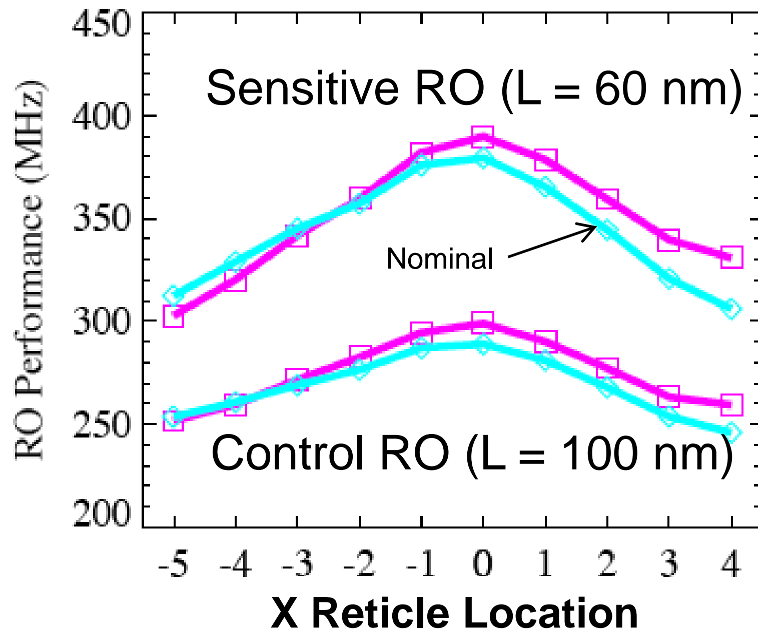
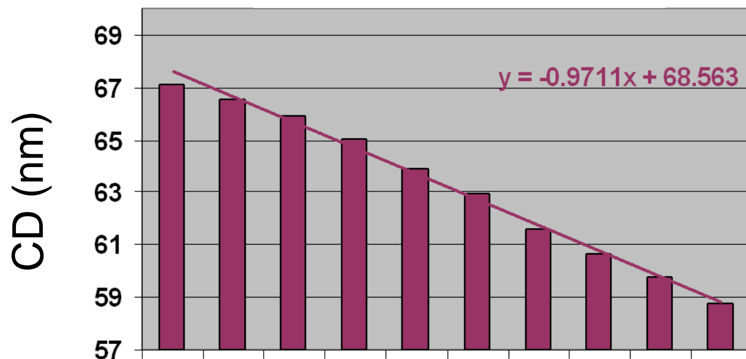
# Decreasing Correlation (continued)

## Poly Dose-Exposure *RO Performance Sensitivity: PBM » Physical CD*




- Striped Exposure Wafer
  - Target Poly CD Variation = -1 nm/stripe
  - CD affect more pronounced on short-channel RO
  - Average Freq. (L=60nm) = 329.2 MHz, 1σ = 32.1 MHz
  - Nominal wafer : Average Freq. (L=60nm) = 308.3 MHz, 1σ = 18.1 MHz
- Across-wafer $L_{EFF}$ variations dominate exposure-induced CD variations



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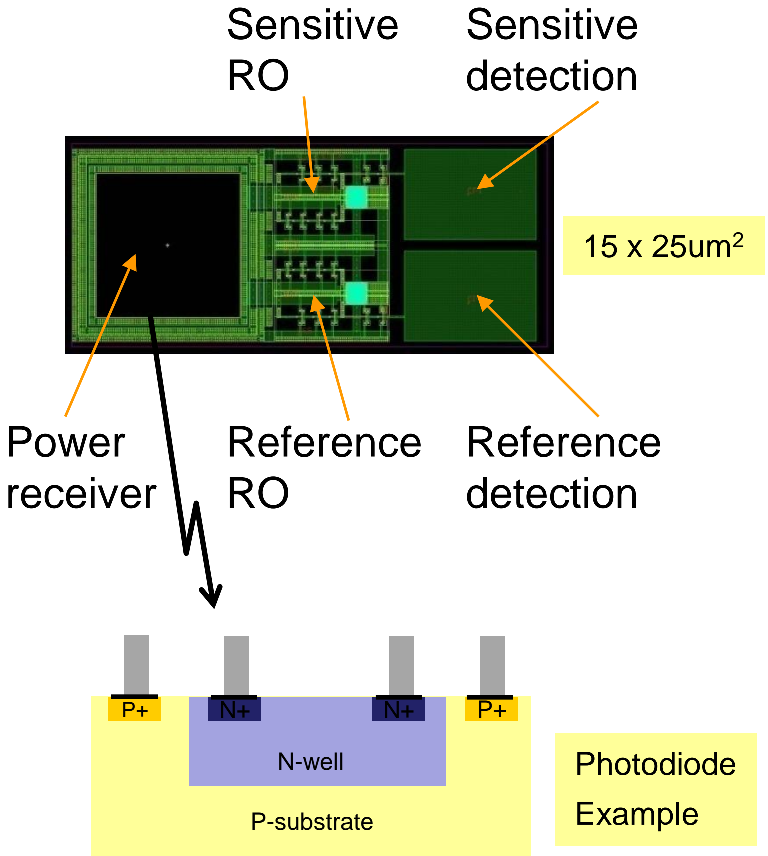
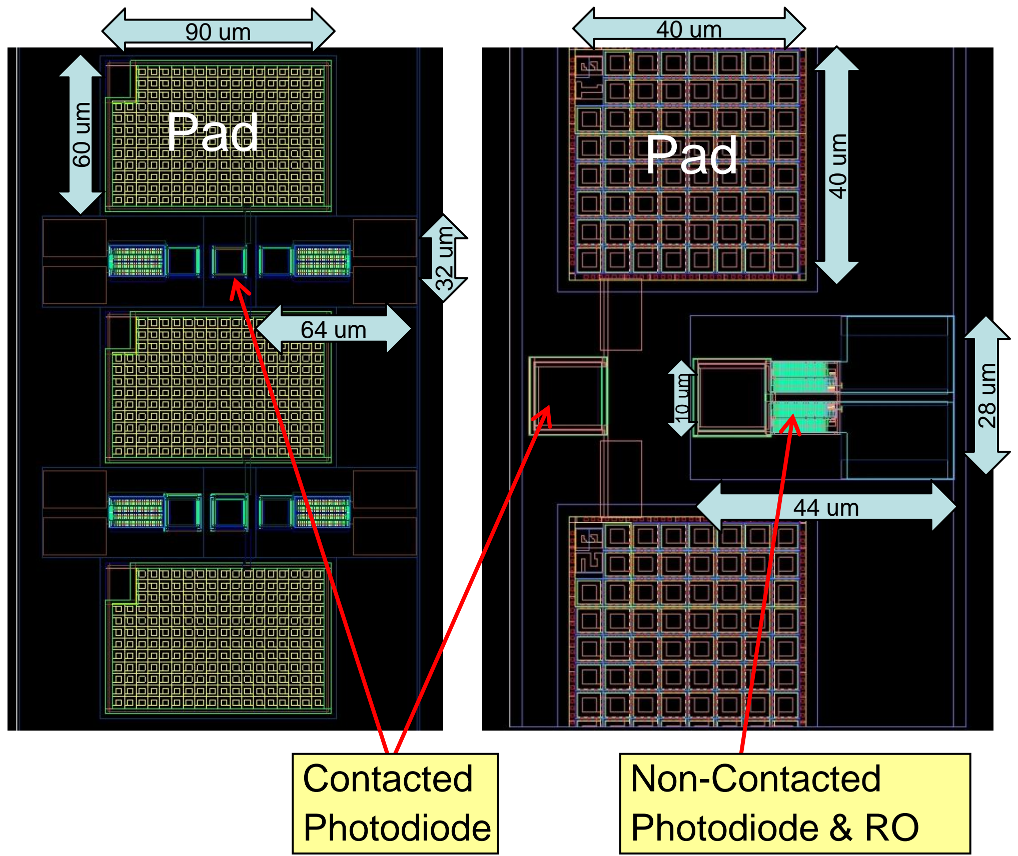
# PBM Basics: Test Block, Photodiode

## Footprint and Layout Examples

- General PBM Test Block:




- Scribe PBM Test Block examples:

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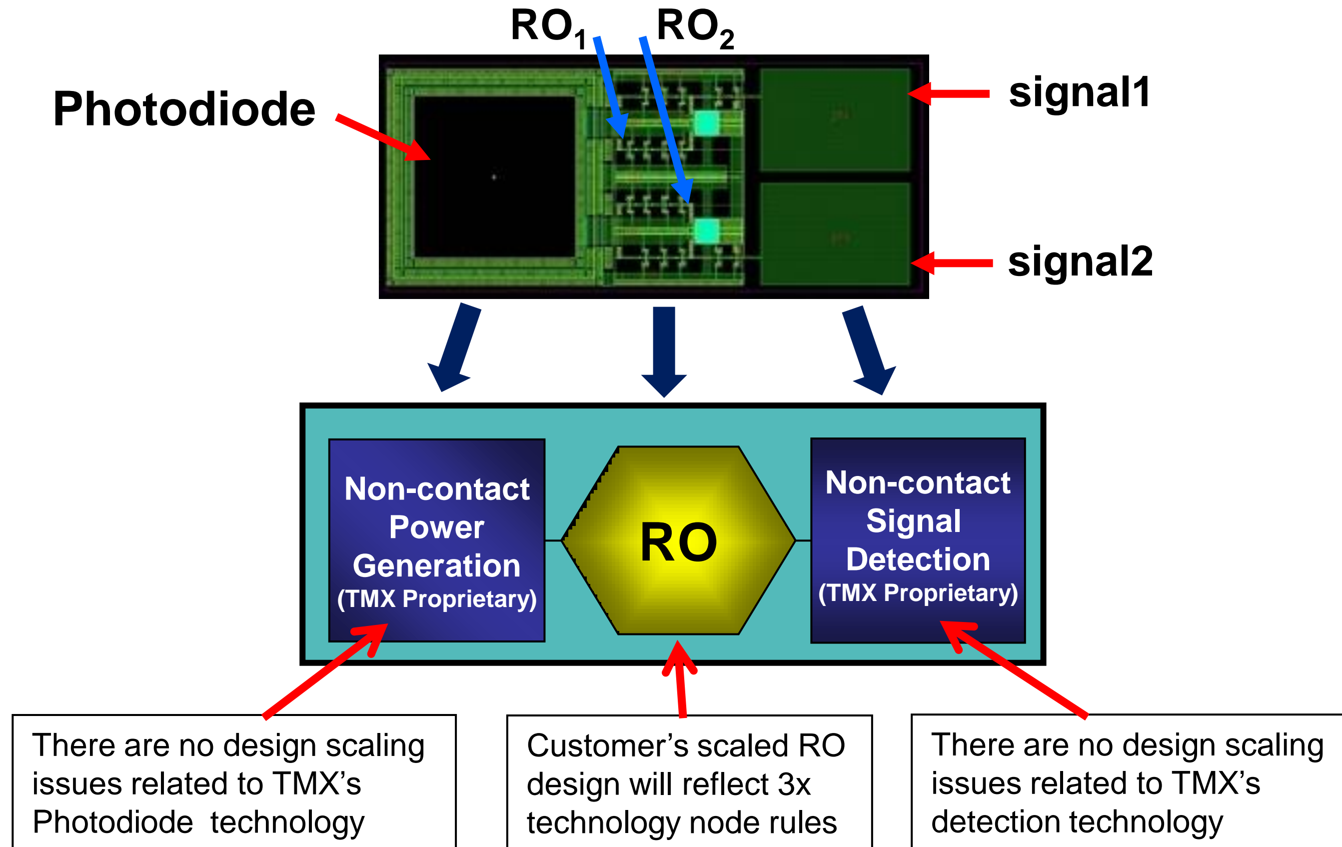
# Scaling PBM to 3X Technology Nodes




- Non-Contact PBM test structures are independent of technology scaling

# Comparison Table:

## *PBM vs. "conventional" techniques for in-die control*

| | Parametric/Scribe | Physical metrology | Final-test | PBM |
|---|---|---|---|---|
| **Correlation to bin-yield** | Scribe to Product die (decreasing) | Very indirect (decreasing) | Direct | Gate/M1-N thru to product test performance correlation |
| **Output (information)** | elec. parametric | Physical dimensional | Product performance specifications | performance time-based, delays (frequency)) |
| **Location & availability** | Scribe area & decreasing | Scribe area & in-die (limited) decreasing | N/A | In-die, product cell size |
| **in-die (product)** | Special masks/flow and/or product integration | yes | yes | yes |
| **Invasive (contact)** | yes | non-contact | N/A | Non-contact and product compatible |
| **Test-Structure foot print limitation** | Pad-size | CD - 10s of microns (i.e. scatterometry) | Product I/O and/or pad contact | Product cell-size macro (25 – 100μm$^2$) |
| **Design Overhead** | MUX & pin-outs | Footprint | BIST | None (placed as product independent design cell) |
| **Learning Cycle (feedback to yield)** | Selective and/or episodic | long turn-around (to final test) | Selective and/or episodic | Immediate |
| **Throughput (measurement per site)** | massively parallel | seconds | massively parallel | under 50ms |



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