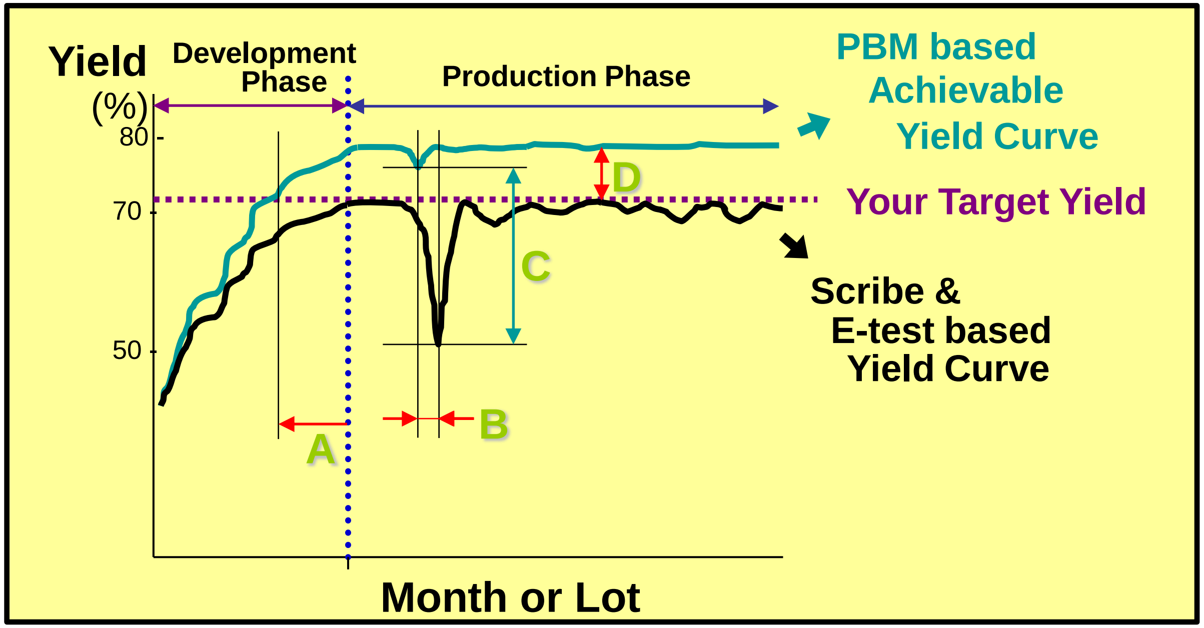
tau-Metrix, Inc.

A Product Yield Enhancement Company



- Enabling our customers to obtain and optimize:
  - **superior** indie product variability learning (early in the flow: metal 1)
  - **faster** product development ramp cycles
  - **enhanced** insight into design-process interactions
  - **improved** performance-based product yield

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Performance-based Metrology™

Value Statement

Non-Contact, Pad-less Characterization Technology

- Industry Problem
  - **Increasing and dynamic offset** between scribe and in-die performance levels
  - **decreasing correlation** between physical metrology and final product performance
  - **costs** for special test-masks, off-line test, and lost product wafers
- The Solution: PBM Technology
  - small-footprint enables **pervasive in-die placements** (in-die variability)
  - autonomous design allows "drop-in" test structures, no wired power, no JTAG
  - enables **early, non-contact performance measurements** of product-representative ckts.
  - enables **continuous across-die, across-wafer, line-line, fab-fab monitoring,** and "contract" verification between design and manufacturing groups
  - **enhanced** process-design interaction **feedback** and improved forecasting of final bin yield
  - **faster product yield ramp** cycles and continuous process control
  - **early intervention** of process excursions to limit impact

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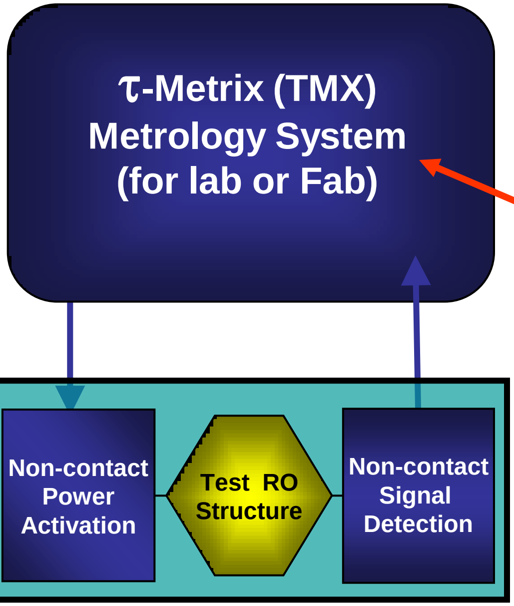
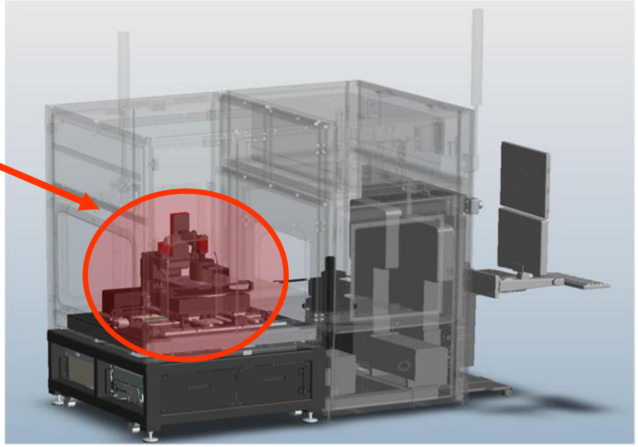
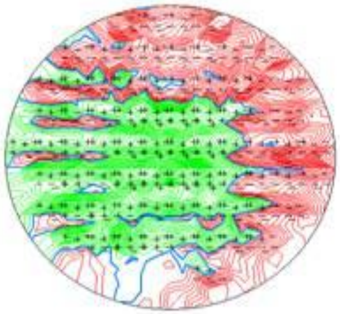
- A pad-less, non-contact, performance-based metrology (PBM) technology
- The PBM technology: 1) measurement tool and 2) on-silicon test design
- Characterization of in-die and across wafer performance variability



On-silicon PBM block (Padless)

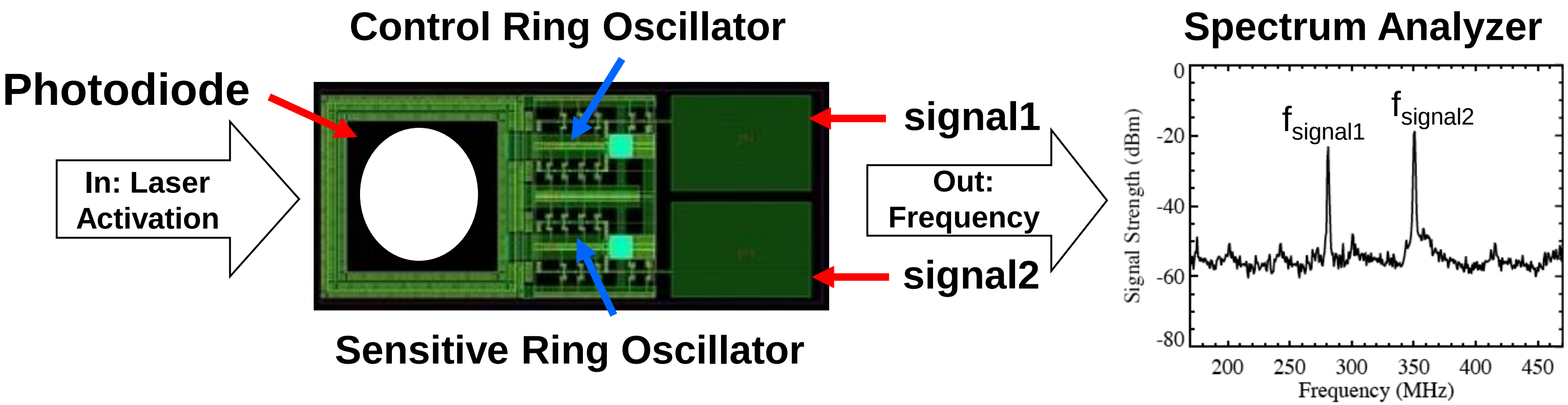


Product Performance Wafer Map at Metal 1



On-Wafer PBM Structure

Small Footprint, Pad-less, Autonomous design



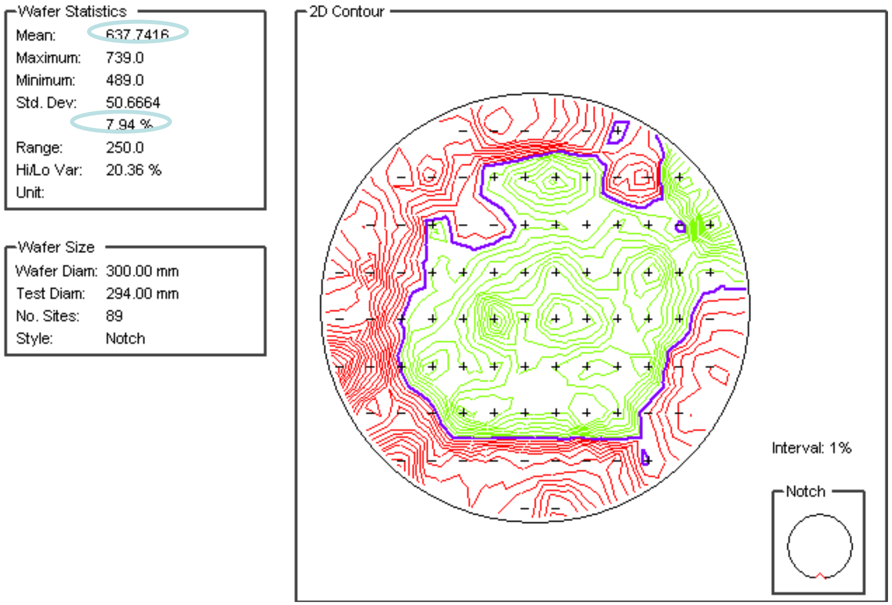
- Small size: ~10 by 20 μm, can be placed in scribe or within product
- Pad-less, no-pin, electrically and functionally "autonomous" design
  - "Wire-less" activation powered and independent of surrounding circuitry
  - Uses standard CMOS design with user's normal process flow
- Differential ROs ("control" and a "sensitive") minimize the impact of:
  - Power supply variations common to both ROs
  - Typical ckts: INV, NAND, NOR, and customer-modified SRAM-based ROs

Standard Probe (contact) vs. PBM (non-contact):

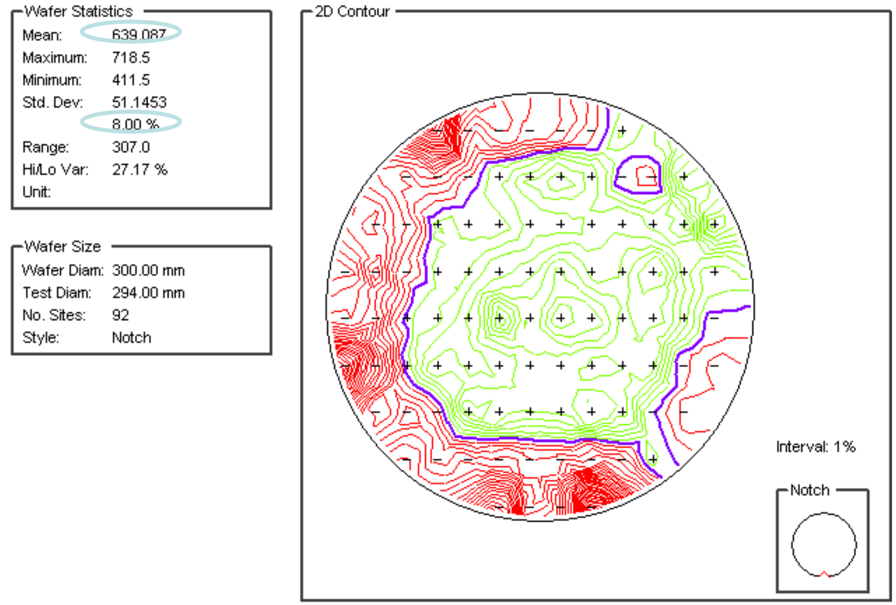
Direct one-to-one Comparison

45-nm SOI Inverter FO=1 RO Results at M2

Probed Measurements



TMX Non-contact Measurements



Results Summary	Probed	Non-contact
Wafer Mean	**637.7 MHz**	**639.1 MHz**
Across Wafer Std. Deviation	**7.94%**	**8.00%**

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Multi-Point In-Die PBM Benefit:

Early, fast, non-destructive/contact, performance measurements to Assess Local (in-die) and Global (wafer-level) Performance Variation

1 measurement site per field

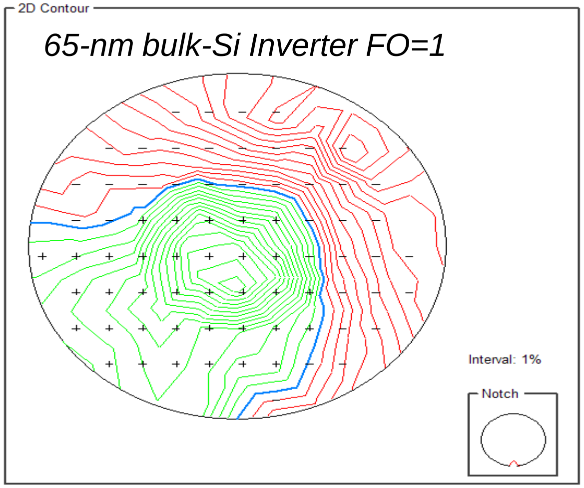
Wafer Statistics

Mean:	292.8518
Maximum:	344.5232
Minimum:	242.1327
Std. Dev:	23.8936
	8.16 %
Range:	102.3905
Hi/Lo Var:	17.45 %
Unit:	

Wafer Size

Wafer Diam:	300.00 mm
Test Diam:	300.00 mm
No. Sites:	74
Style:	Notch

Scribe-like, single point PBM data



Drawn Gate: 60 nm

292 MHz 17.5%

8 measurement sites per field

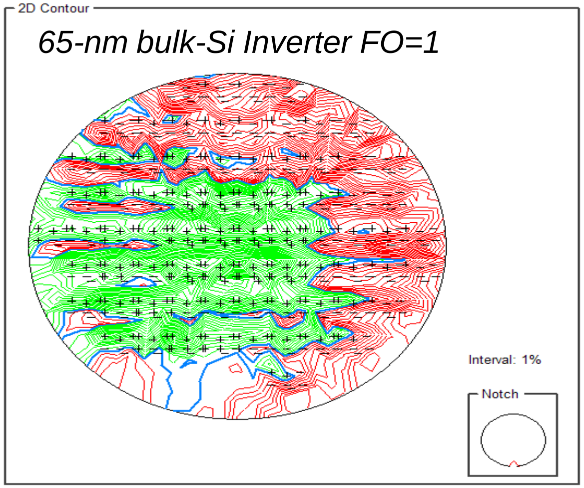
Wafer Statistics

Mean:	292.8517
Maximum:	389.2375
Minimum:	206.8667
Std. Dev:	31.972
	10.92 %
Range:	182.3708
Hi/Lo Var:	30.59 %
Unit:	

Wafer Size

Wafer Diam:	300.00 mm
Test Diam:	300.00 mm
No. Sites:	518
Style:	Notch

Multi-point PBM data



Drawn Gate: 60 nm

292 MHz **30.6%**

- **Single point/scribe measurements and physical metrology do not sufficiently capture across chip variation (ACV) contribution to in-die performance variation**
- **Key in-die process sensitivities are missed with conventional scribe measurements**

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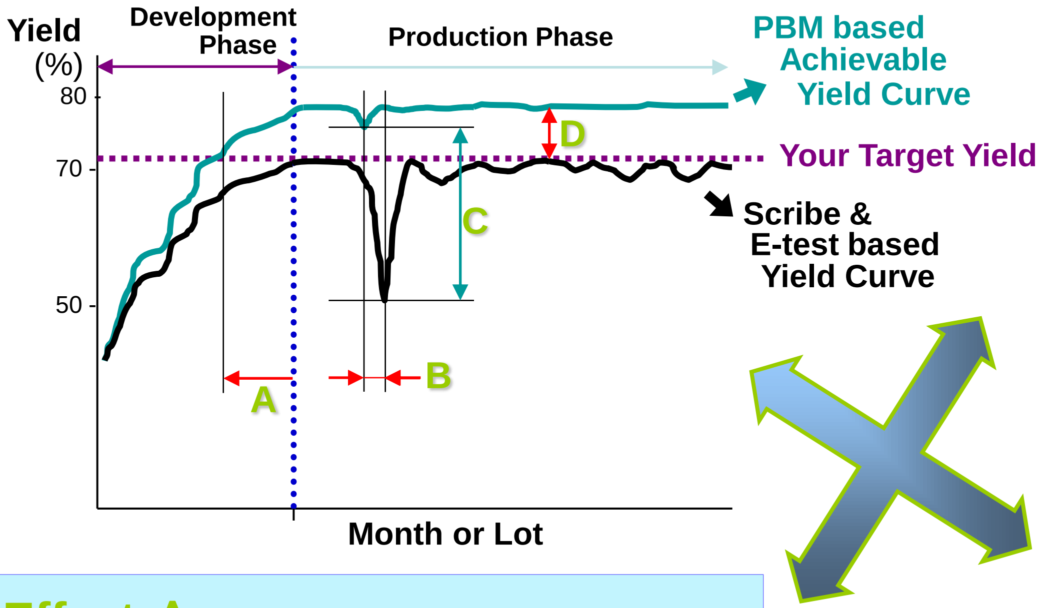
Performance-Based Metrology (PBM)
Applications

- Early Technology Development Phase:
  - Quick-cycle device/process characterization
  - Process (V_t, L_{poly}, Rx, anneal) sensitivity learning
  - Health-of-line, ACLV, Local and Global tracking assessment
  - Improved feedback for design rules and models (ACV, etc.)
- Product Ramp and Production Phase:
  - Improved ROI
  - Quicker Design-Process interaction feedback
  - Accelerated product-yield ramp
  - Continuous monitoring of in-die performance metrics

PBM Yield Improvement

Time-Dependent (Product Dev./Ramp) and Final



Effect B & C :

tau-Metrix PBM technology provides process variation monitoring in timely manner. Deep yield-loss excursions will be minimized with very short TAT, which obviates the wait time (delay) for E-test results.

Cost Savings !!!

Effect A :

tau-Metrix PBM technology provides performance-based measurement data at M1. It helps to manage both process variation and yield. It is also an enabler to achieve product yield targets earlier than the conventional schemes, which minimizes lead time.

Time to Market !!!

Effect D :

tau-Metrix PBM technology collects in-die process variation data at M1. It can monitor and improve process continuously, which can accelerate production cycle times. The early and enhanced learning can improve and maintain higher final yield levels.

Increase Revenue !!!

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ROI

MPU Example (Yield Improvement + Bin Allocation Shift)

Fab Balance Sheet, per Month		
Wafer Production Costs	Standard Metrology	Performance-Based Metrology
@ M1	$1,500.00	$1,500.00
@ MF	$2,500.00	$2,500.00
Wafer Starts	30000	30000
Wafers Pulled @ M1 for Test	300	30
Reticles per Wafer	74	74
Die per Reticle	4	4
Failing Product	30%	25%
Bin 2 Product Yield	50%	40%
Bin 1 Product Yield (best perf.)	20%	35%
Good Die Produced	6,153,840	6,653,340
Fab Costs ($M)	$74.7	$75.0
Cost per Good Die	$12.14	$11.27
Manufacturing Savings	--------------->	-7.17%
Bin 2 Product Value	$80.00	$80.00
Bin 1 Product Value (best perf.)	$140.00	$140.00
Product Revenue ($M)	$597.8	$718.6
Gross Profit ($M)	$523.1	$643.6
Increased Monthly Profit ($M)	--------------->	$120.5

Note: Improvement in product-yield ramp (in time) is not incorporated in this analysis

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