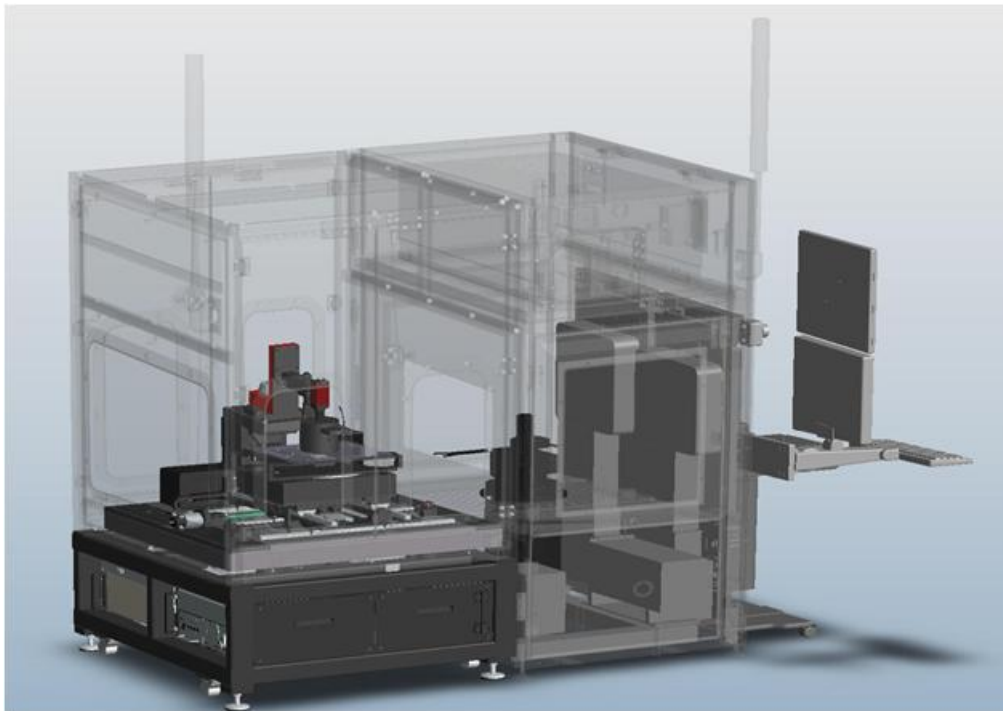


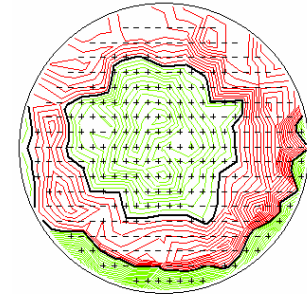
τ -Metrix, Inc.

Performance Based Metrology (PBM)

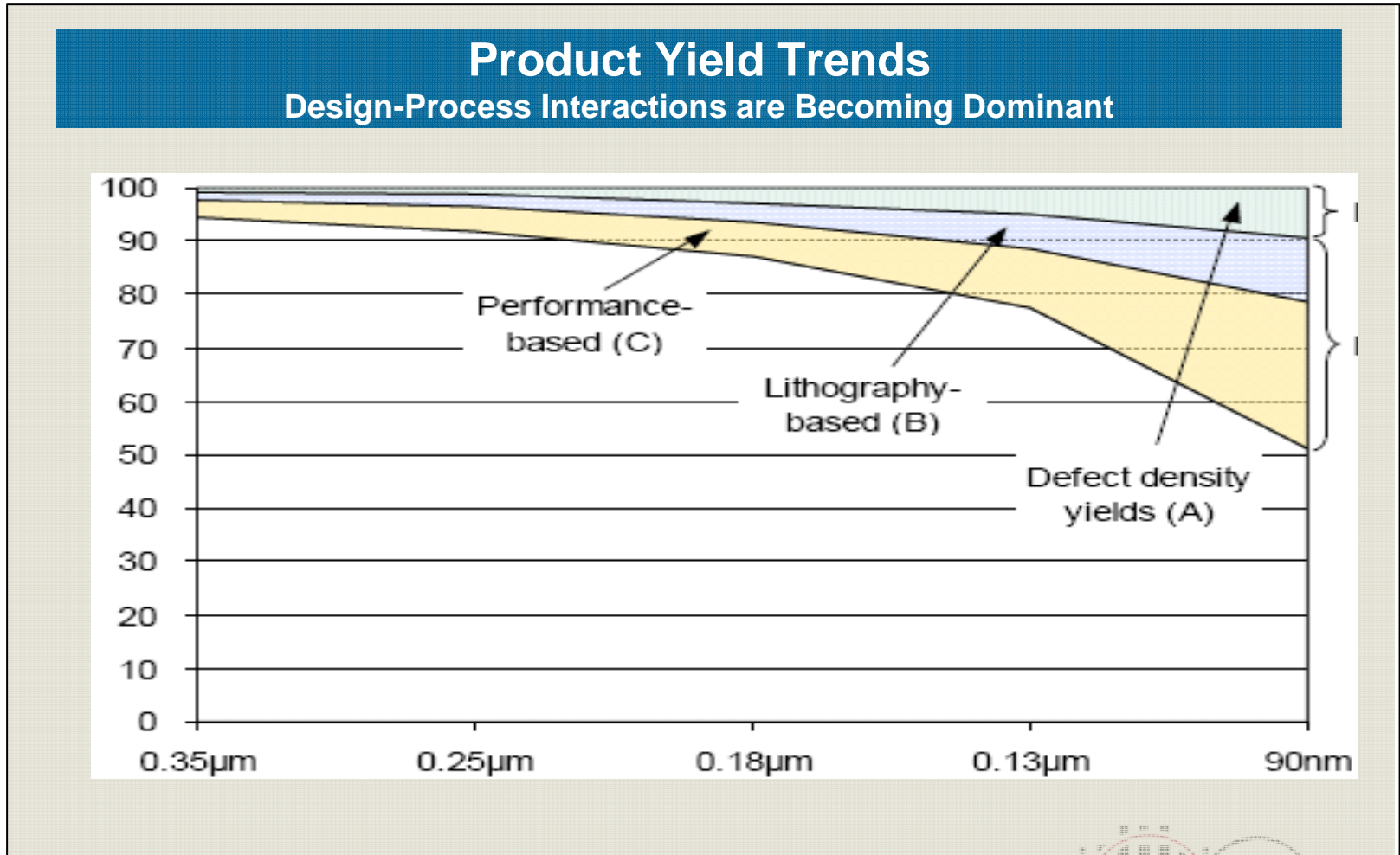
Enabling non-contact in-die and pad-less measurements of product performance throughout technology development and production cycles



Product Performance
Wafer Map at Metal 1



In-die Variability as the Fastest Growing Yield-Limiter



Automated Optoelectronic Metrology System with Proprietary Non-Contact Power & Signal Detection Targets

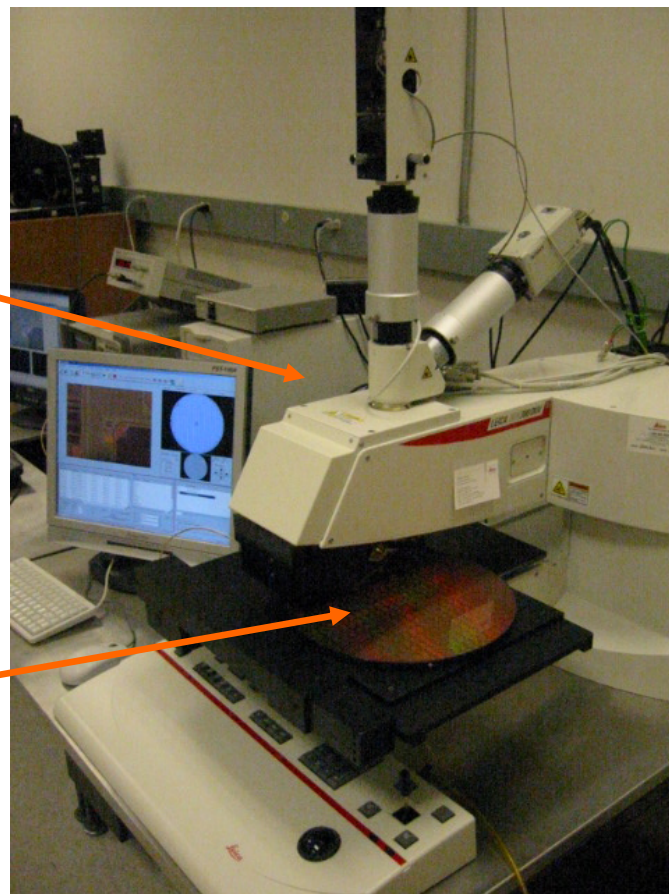
τ -Metrix (TMX)
Metrology System
(for lab or Fab)

Active device
test-structure
(TMX proprietary or
customer design)

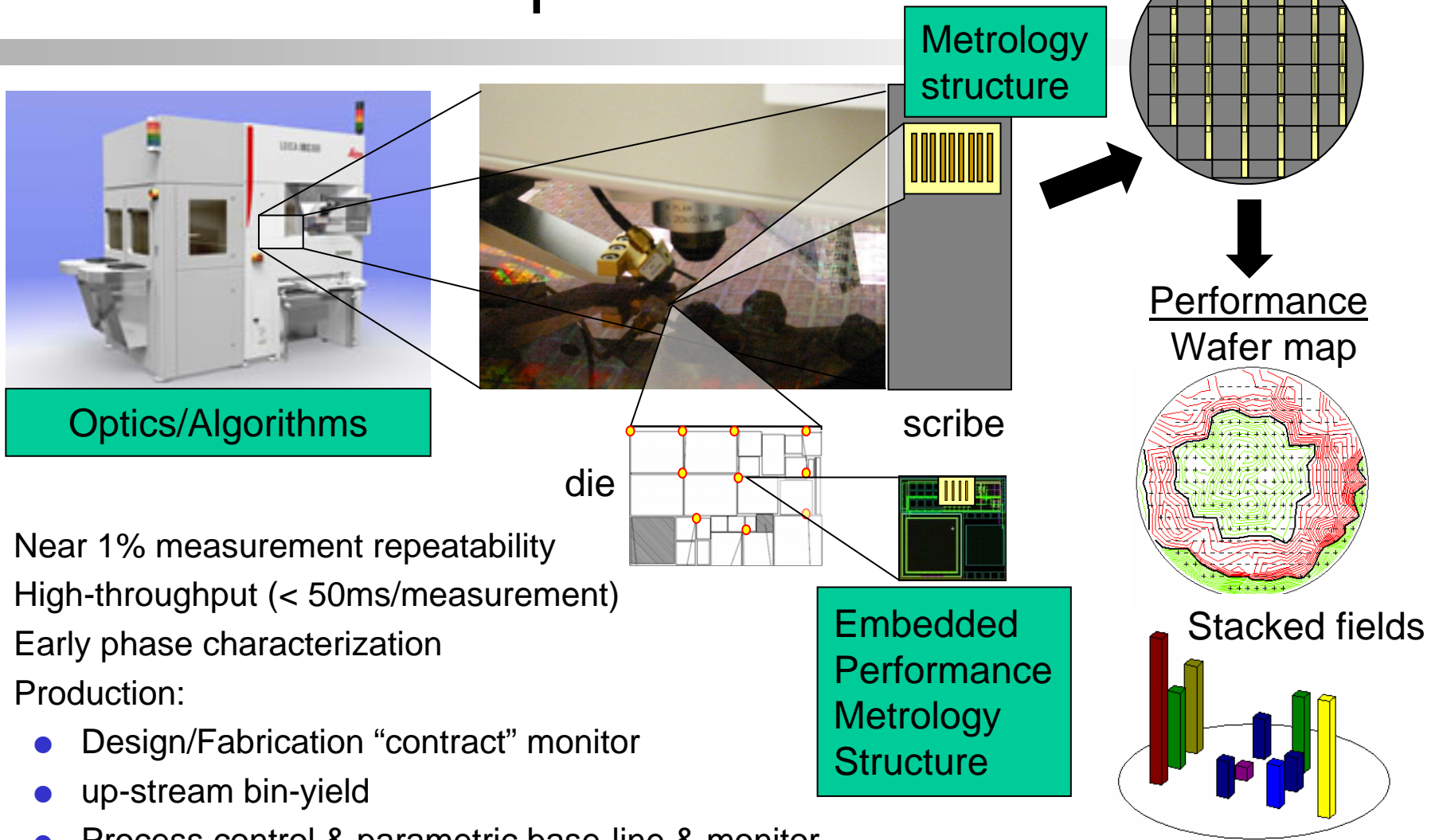
Non-contact
Power
Generation
(TMX Proprietary)

Non-contact
Signal
Detection
(TMX Proprietary)

On-silicon PBM block (Padless)



PBM Couples Metrology with its Performance Impact



- Near 1% measurement repeatability
- High-throughput (< 50ms/measurement)
- Early phase characterization
- Production:
 - Design/Fabrication “contract” monitor
 - up-stream bin-yield
 - Process control & parametric base-line & monitor

Performance Based Metrology: *Applications*

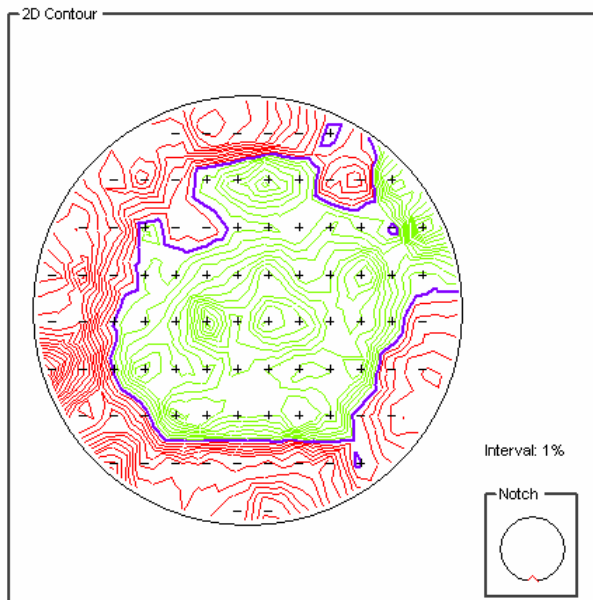
- **Early Technology Development Phase:**
 - Quick-cycle device/process characterization
 - Process (Vt, Lpoly, Rx, anneal) sensitivity learning
 - Health-of-line, ACLV, Local and Global tracking parametrics
 - Improved feedback for design rules and models
- **Product Ramp and Production Phase:**
 - Fab-design integration & monitor
 - Prediction of final bin yield from M1 silicon
 - Process control
 - Yield ramp
 - Bin-yield control & optimization
- **FA/diagnostics**

Standard Probe vs. non-contact PBM: 45-nm SOI Inverter FO=1 RO Results at M2, 1A Diode

Probed Measurements

Wafer Statistics	
Mean:	637.7416
Maximum:	739.0
Minimum:	489.0
Std. Dev:	50.6664
	7.94 %
Range:	250.0
HiLo Var:	20.36 %
Unit:	

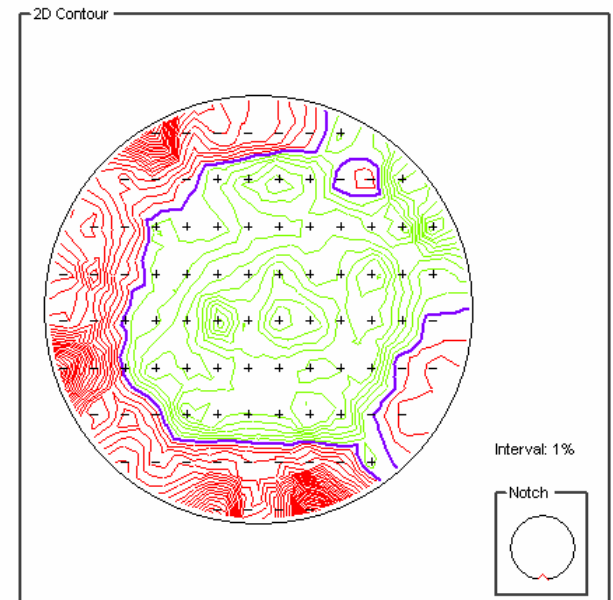
Wafer Size	
Wafer Diam:	300.00 mm
Test Diam:	294.00 mm
No. Sites:	89
Style:	Notch



TMX Non-contact Measurements

Wafer Statistics	
Mean:	639.087
Maximum:	718.5
Minimum:	411.5
Std. Dev:	51.1453
	8.00 %
Range:	307.0
HiLo Var:	27.17 %
Unit:	

Wafer Size	
Wafer Diam:	300.00 mm
Test Diam:	294.00 mm
No. Sites:	92
Style:	Notch



Results Summary	Probed	Non-contact
Wafer Mean	637.7 MHz	639.1 MHz
Across Wafer Std. Deviation	7.94%	8.00%

Advantages of PBM In-line Non-Contact Technology

■ PBM Enables

- across-die, across-wafer, line-line, & Fab-Fab monitoring and “contract” verification between design and manufacturing groups
- improved prediction of final bin yield using in-die measurements as early as M1

■ PBM Addresses

- increasing offset between scribe and in-die performance levels
- decreasing correlation between physical metrology and final product performance
- costs for special test-masks, off-line test, and lost product wafers

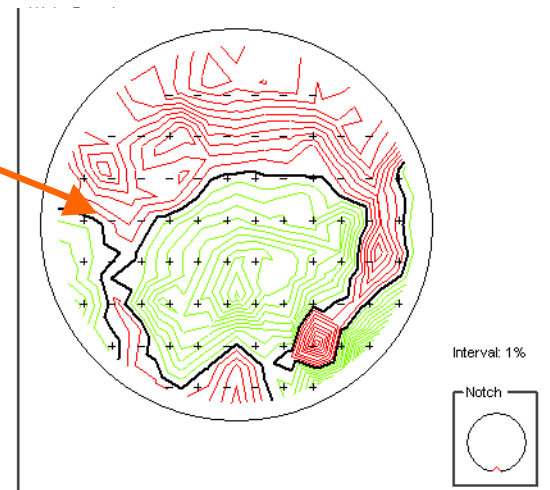
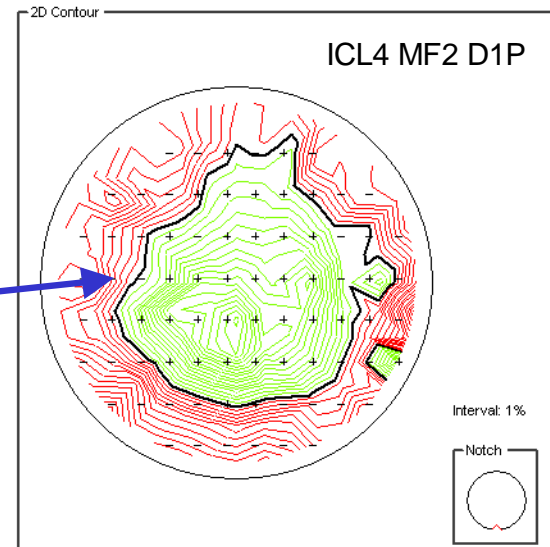
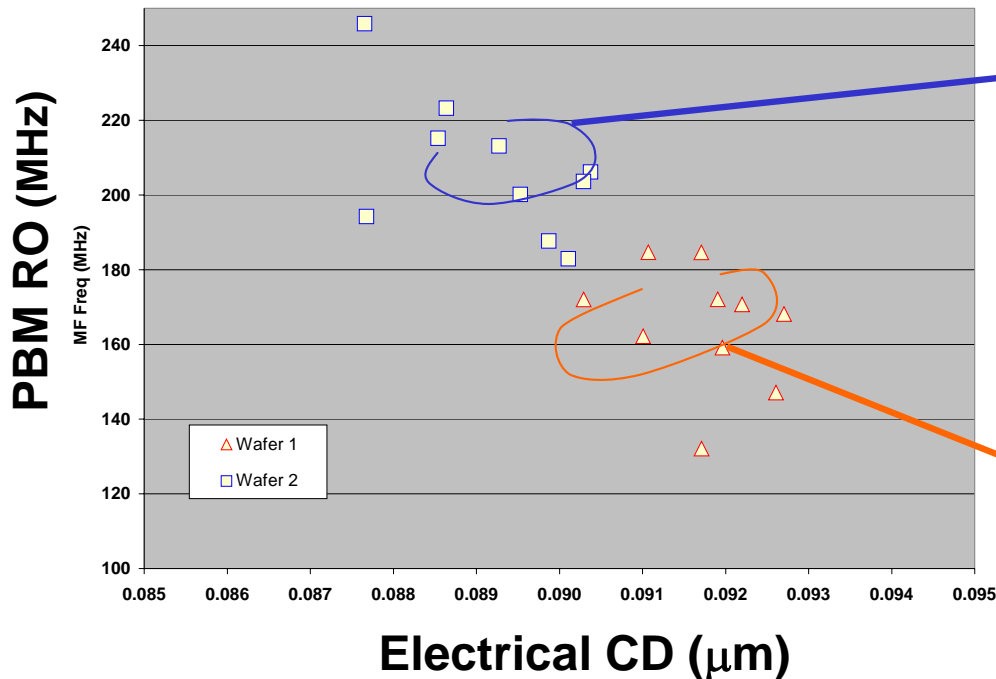
■ Backup Slides

- Results
- Comparison Table

PBM Link with Standard Metrology

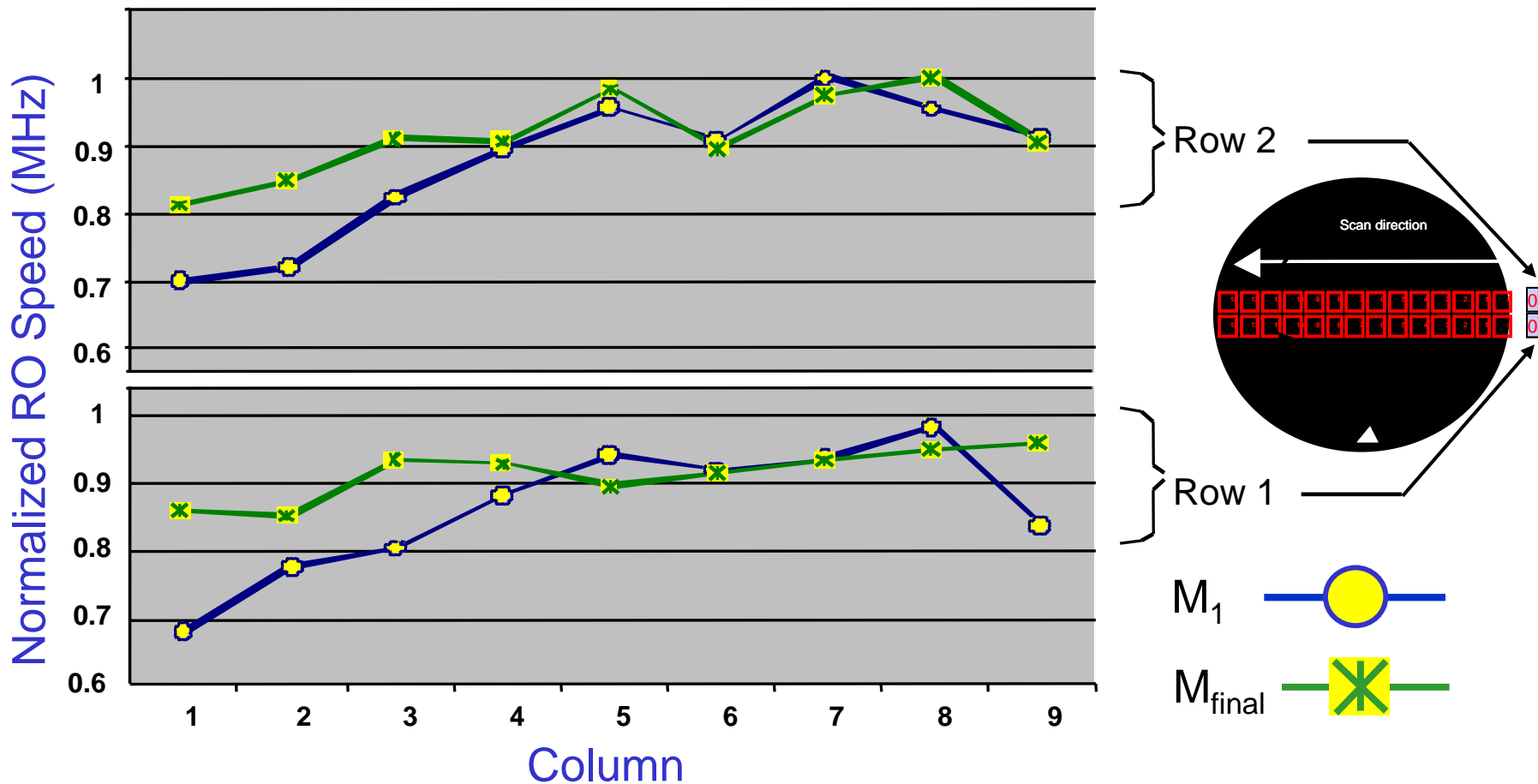
Non-contact measurements correlate to eCD

- In-die mapping reveals process fingerprint & identified slower wafer, 15% decrease in speed**



Source: Tau-Matrix/ST/Philips/Freescale, SPIE 2006

“Upstream” bin-yield: PBM M_1 results forecast M_{final} behaviour



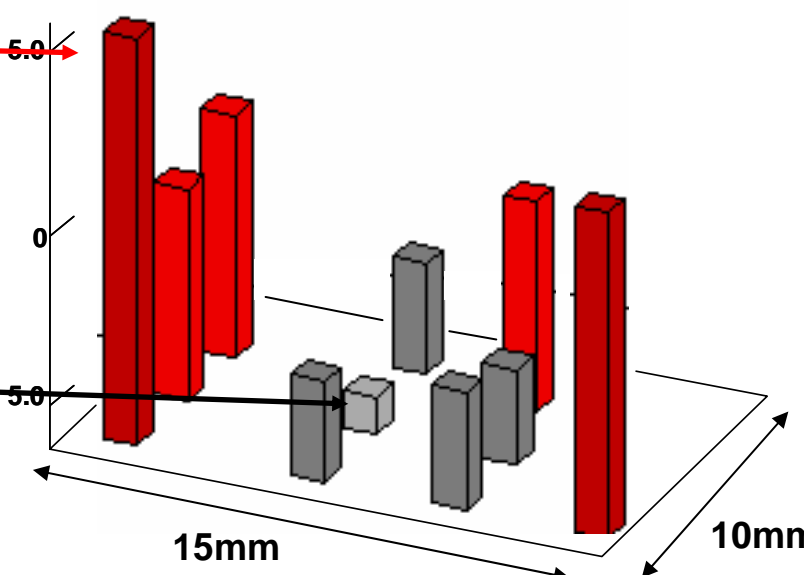
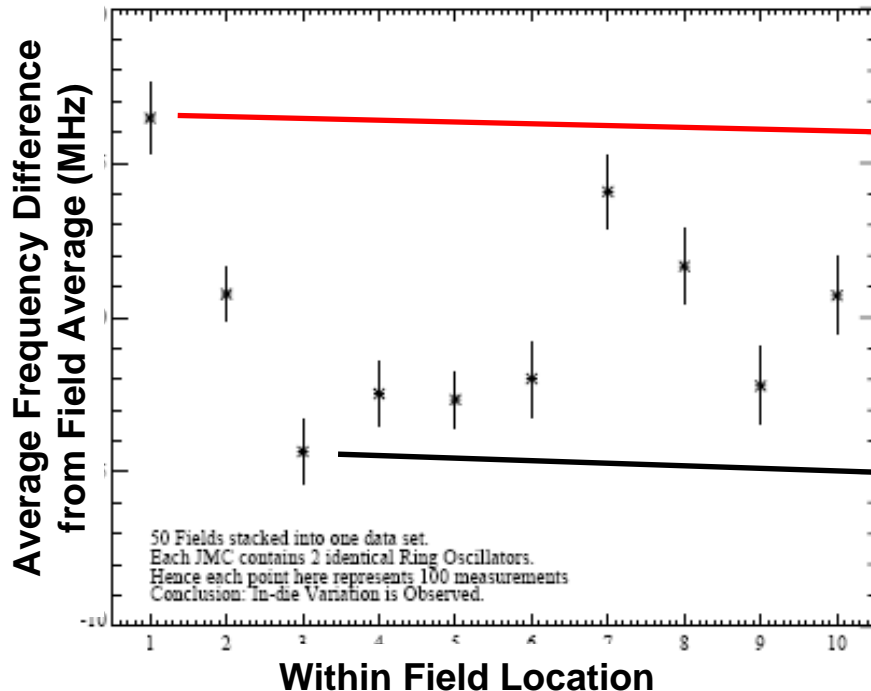
Source: tau-Matrix/ST/Philips/Freescale, SPIE 2006

PBM → ACV mapping

Non-contact measurements of in-chip Ring Oscillators

Few % residual ACV invisible to scribe-based metrology

Wafer Stack within Field Variation



Non-contact measurements performed on 90nm process

Source: tau-Metrix/ST/Philips/Freescale, ASMC 2006

Multi-Point PBM Benefit:

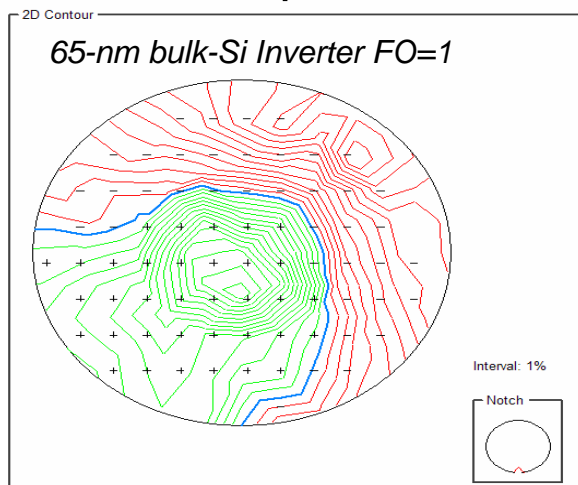
Superior Local and Global Variation Assessment Capability

1 measurement site per field

Wafer Statistics	
Mean:	292.8518
Maximum:	344.5232
Minimum:	242.1327
Std. Dev:	23.8936
Range:	8.16 %
Hi/Lo Var:	102.3905
Unit:	17.45 %

Wafer Size	
Wafer Diam:	300.00 mm
Test Diam:	300.00 mm
No. Sites:	74
Style:	Notch

Scribe-like,
single point
PBM data



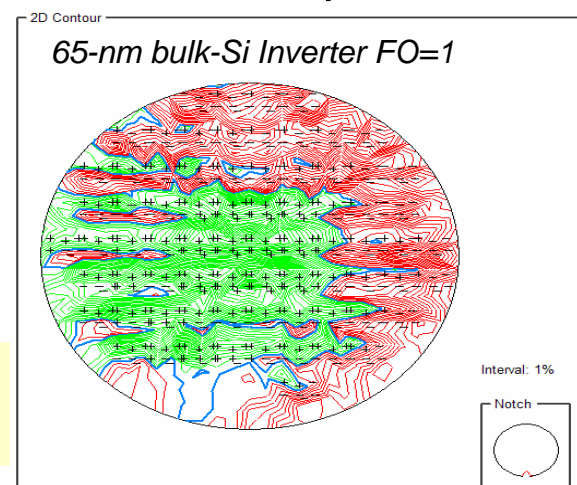
Drawn Gate: 60 nm
292 MHz \pm 17.5%

8 measurement sites per field

Wafer Statistics	
Mean:	292.8517
Maximum:	389.2375
Minimum:	206.8667
Std. Dev:	31.972
Range:	10.92 %
Hi/Lo Var:	182.3708
Unit:	30.59 %

Wafer Size	
Wafer Diam:	300.00 mm
Test Diam:	300.00 mm
No. Sites:	518
Style:	Notch

Multi-point
PBM data



Drawn Gate: 60 nm
292 MHz \pm **30.6%**

Single point/scribe measurements do not capture across chip variation (ACV) contribution to final performance variation

Comparison Table:

PBM vs. “conventional” techniques for in-die control

	Parametric/Scribe	Physical metrology	Final-test	PBM
Correlation to bin-yield	Scribe to Product die (decreasing)	Very indirect (decreasing)	Direct	Gate/M1-N thru to product test performance correlation
Output (information)	elec. parametric	Physical dimensional	Product performance specifications	performance time-based, delays (frequency))
Location & availability	Scribe area & decreasing	Scribe area & in-die (limited) decreasing	N/A	In-die, product cell size
in-die (product)	Special masks/flow and/or product integration	yes	yes	yes
Invasive (contact)	yes	non-contact	N/A	Non-contact and product compatible
Test-Structure foot print limitation	Pad-size	CD - 10s of microns (i.e. scatterometry)	Product I/O and/or pad contact	Product cell-size macro (25 – 100 μ m ²)
Design Overhead	MUX & pin-outs	Footprint	BIST	None (placed as product independent design cell)
Learning Cycle (feedback to yield)	Selective and/or episodic	long turn-around (to final test)	Selective and/or episodic	Immediate
Throughput (measurement per site)	massively parallel	seconds	massively parallel	under 50ms

PBM Implementation Strategy

Test Structures and Timeline

■ Test Structures:

- Need all-layer mask revision (through M1 at least)
- Product or Test Chip design implementations
- Scribeline variants:
 - Non-contact Photodiode, RO, detector
 - Contacted and Isolated photodiode, RO
- In-die variants:
 - Non-contact Photodiode, RO (low, medium, high power), detector
- Contacts (design/mask, process integration, test, product engineering)

■ Timeline (Example):

Week 0-2	Week 1-2	Week 3-4	Week 4	Week 4-8	Week 8-12	Week 13-14
Technology Description (RO, diode, design rules) Owner: USER	Scribe (and in-die) PBM block Owner: TMX	PBM block implementation Owner: USER	Review & Release Owner: ALL	Product tapeout Owner: USER	Silicon processing/fabrication Owner: USER	Measurements & Analysis Owner: ALL