Non-Contact, Pad-less Measurement Technology and Test Structures for Characterization of Cross-Wafer and In-Die Product Variability

Gary Steinbrueck, James S. Vickers, Majid Babazadeh, Mario M. Pelella, and Nader Pakdaman
tau-Metrix Inc., Santa Clara, CA
gs@tau-metrix.com

Abstract:

Monitoring and controlling cross-wafer and in-die variability have been recognized as the dominant and escalating factors for the successful commercialization of modern-day integrated circuit products utilizing advanced semiconductor manufacturing[1,2]. In this paper we present a performance based metrology (PBM) and measurement technology to further close the information gap that currently exists between the design, process integration, and manufacturing to control variability.

PBM enables the "porting" of scribe-like and end-of-line contacted measurements to within the product's active die while it provides the capability to significantly reduce the cycles of learning to obtain relevant and key process, device, and product metrics. This product-relevant information can then be used for process monitoring and control, performance optimization, and to enhance early bin-yield predictability. The technique would reduce or eliminate the need for send-ahead test wafers and other "disruptive" measurements by making possible in-die, noncontact characterization of product performance monitors and devices.

The paper will describe the design and implementation considerations of the non-contact test structures on product wafers, and the details of the in-line PBM measurement system. Experimental results from PBM measurements on several generations (90, 65, and 45nm) of bulk-Si and SOI product wafers and devices will presented and discussed.

1. Introduction to PBM

PBM allows the measurement of in-die variability on product-like test structures at the early stages of manufacturing when first circuit connectivity is realized (i.e. 1st metal). This "early" information can be used to monitor and control performance variation for line-to-line (L2L), run-to-run (R2R), wafer-to-wafer (W2W), and die-to-die (D2D) design/product/process monitor and control.

The need to complement and manage the critical and yet traditional metrology techniques with parametric-line, in-die measurement which correlate directly to final-performance and ultimately (performance) bin-yield has been recognized in detail[3]. PBM accelerates the gathering and availability of the current critical measurements of product representative[4] RO-type test structures in the scribe and die[5] from early stages of product development and continuously throughout the manufacturing process steps and phases. This is achieved with laser-facilitated, contact-less "power/probe pads" that enable the non-contact measurement of the product-like ROs in the active product die and scribe.

The paper/presentation will begin with an introductory section to outline the industry trends that require the critical need of controlling variability for every phase of productization of advanced products. We will then introduce the PBM architecture with the design considerations for its implementation on product, followed by experimental results that show the capability of this novel technique.

These results are meant to demonstrate how PBM could be used to extend the capabilities of current in-line, in-die parametric practices to measure and control variability and enhanced bin yield predictability, very early in the process flow. The results will also illustrate that a broad utilization of PBM's test structures could be implemented from early-technology development through product ramp and full production to provide continuity of the process, transistor, and performance metrics and as an early "base-line" for process control and optimization adjustments.

2. Performance based metrology (PBM): Architecture

The PBM system encompasses two functional blocks: 1) the non-contact power delivery and measurement component; 2) the embedded (in product silicon) structures to enable the noncontact activation (power) and measurement of the product-representative test structures.

The overall system architecture has been captured in Figure 1. The measurement component is comprised of an automated wafer movement and handling system, along with the associated imaging system to enable fast alignment and positioning. The power delivery and coupling to the power-structure on the silicon and the signal detection rely on optoelectronic effects and devices.

3. Pad-less non-contact power & signal detection design and integration to ROs

Test structures, which are comprised of ring oscillators and power/sense devices (Figure 2), are formed with standard product mask layers and process steps - no additions and/or modifications to the standard product definition and associated fabrication process is needed. Integration into product or scribe requires adherence to standard design rules and/or definition of special device types for compatibility with production design checkers. Non-contact signal sense is provided by optical or capacitive pickup. The source of power is a laser stimulated photodiode. This means that optical access to the silicon layers is required up to the time of measurement. Within these ground rules, a large variety of information can be obtained and related directly to device parametric, process, and product variability. In the normal context of yield management this data can be interpreted in combination with that from other sources to provide very early feedback with no scrap or special run cost.

Ring oscillators (ROs) specifically designed for process centering and monitoring of variability have provided a direct link to contact measured parameters on product wafers[6]. It is especially advantageous that the same product-like RO design can now be

placed in-die with functional and electrical independence of any product structures or interconnect. Design of the equivalent noncontact structures involves only removal of control and frequency converters, adjustment for period and power, and addition of non-contact sense/power devices.

The standard RO can be extended with designs sensitive to particular process variations. These can be device related: effective channel length variation (ACLV), local random fluctuation, drive strength, threshold, for example. They can also be designed and placed to show lot, wafer, and die variability of more process specific information: gate/channel overlap (COV), pattern density and other exposure effects, interconnect (geometric, electrical, and delay) variability.

With somewhat more demand on in-die placement, ROs can be fashioned from arbitrary segments of product logic that mimic critical paths in both function and physical design. These can use any level of interconnect, as long as the power/sense structures have optical clearance to the surface of the wafer at the time they are measured. It is even possible to repeat measurements of any targets at subsequent process steps if this requirement is met.

In addition to optical clearance at the time of measurement, the main design requirements for the test targets are: assuring adequate power and current and using standard masks and process steps, designing for appropriate operating frequencies, and verifying the behavior of the designs through model and hardware validation.

4. Experimental Results

The immediate question for the user is to ascertain how closely correlated and representative are the PBM results with the contact measurements performed at test (end-of-line) or the scribe (inline) measurements of the same structures and libraries. In Figure 3A the comparison of results from probed structures versus those obtained from the same structure using the non-contact power/signal structure are demonstrated in a scatter plot. These results, drawn from a 45nm SOI product wafer, demonstrate the near one-to-one correlation between the mechanically probed measurements and those from PBM. Figure 3B demonstrates the same results on a wafer map, and it includes the key statistical data, where the mean and distribution of the contact vs. noncontact (PBM) measurements are compared and demonstrate near one-to-one correlation.

Figure 4 shows the close correlation between electrical CD (eCD) measurements and those using the same samples' (in RO test-structures) measured with PBM on two separate wafers from the same "wafer run". PBM identified the slower (larger eCD) wafer from the "faster" wafer (smaller eCD). For each wafer a close correlation between each site and associated CD was also realized. These results show that PBM could replace eCD with measurements on actual product-like structures (versus the resistivity measurements on poly-lines typically used for eCD) and, in turn not only ascertain and control the wafer's patternng processes, but also provide a direct measure of the effective channel length (L_{eff}) – which in turn provides information on the actual physical and electrical construct and constituents of the gate.

Figure 5 demonstrates the comparison between single site (per-die) measurements versus multisite (in-die) measurement on a multi-product wafer (MPW). The single measurements could be viewed as scribe-like results, whereas the multi-site wafers indicate the in-die variability that is ultimately and directly related to bin-yield. The average (mean) is the same between the two measurements, where as the distribution of the results show a 75% increase in variability.

5. Conclusion

A pad-less, non-contact CMOS circuit performance-based measurement system and technology that enables the monitoring and control of process induced variability across wafer and within the product die has been described. The measurement system includes the design and implementation of non-contact power activation and signal detection structures on product silicon that enable copious characterization of product-representative and process sensitive test-structures.

Experimental results between the non-contact and contacted-probe measurements are in very good agreement for both bulk-Si and SOI scaled technologies. These results indicate that the non-contact performance-based measurement technique is robust and can be utilized in manufacturing lines to directly measure in-die, cross wafer, and cross-line variability. By adopting this technique, critical early learning and visibility of bin-yield from 1st connectivity levels is afforded, well before final test and without the need for send-ahead or uniquely designed mask silicon that impact the manufacturing line's WIP and resources.

1 Duane S. Boning, Karthik Balakrishnan, Hong Cai, Nigel Drego, Ali Farahanchi, Karen Gettings, Daihyun Lim, Ajay Somani, Hayden Taylor, Daniel Truque, Xiaolin Xie, "Variation", *Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED) 2007,* pp. 15-20.

2 Sharad Saxena, Christopher Hess, Hossein Karbasi, Angelo Rossoni, Stefano Tonello, Patrick McNamara, Silvia Lucherini, Seán Minehane, Christoph Dolainsky, and Michele Quarantelli, "Variation in Transistor Performance and Leakage in Nanometer-Scale Technologies", IEEE *TRANSACTIONS ON ELECTRON DEVICES*, vol. 55, no. 1, pp. 131-143, Jan. 2008.

3 A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N. Le, P. Lindo, A. P. Mahorowala, H.-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas and H. Utomo, "Improving the Power-Performance of Multicore Processors Through Optimization of Lithography and Thermal Processing", *Proc. of SPIE,* vol. 6521, pp. 65210K, 2007.

4 Mark B. Ketchen, Manjul Bhushan, "Product-representative 'at speed' test structures for CMOS characterization", *IBM Journal of Research and Development*, vol. 50, no. 4/5, pp. 451-468, 2006.

5 Kelin J. Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Wei-kai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, and Keith Zawadzki, "Managing Porcess Varaition in Intel's 45nm CMOS Technology", *Intel technology Journal*, vol.12, no.2, pp. 93-109, 2008.

6 Bhushan, M. Gattiker, A. Ketchen, M.B. Das, K.K. , "Ring oscillators for CMOS process tuning and variability control", *IEEE Transactions on Semiconductor Manufacturing,* vol. 19, no. 1, pp. 10-18, Feb. 2006.

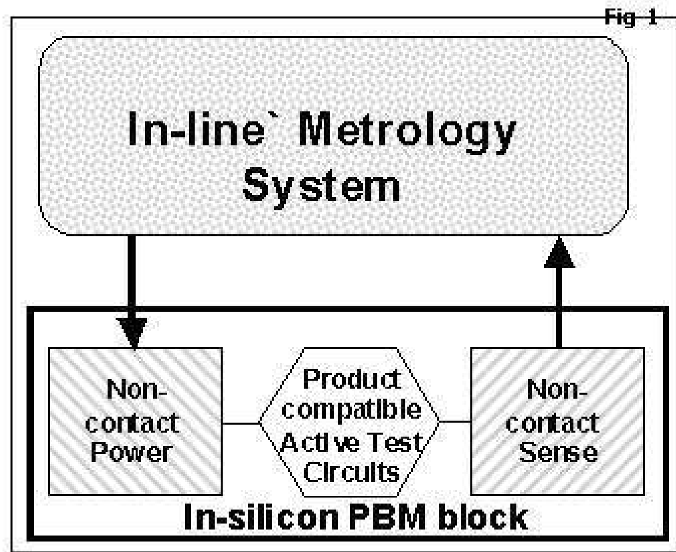


Fig 1

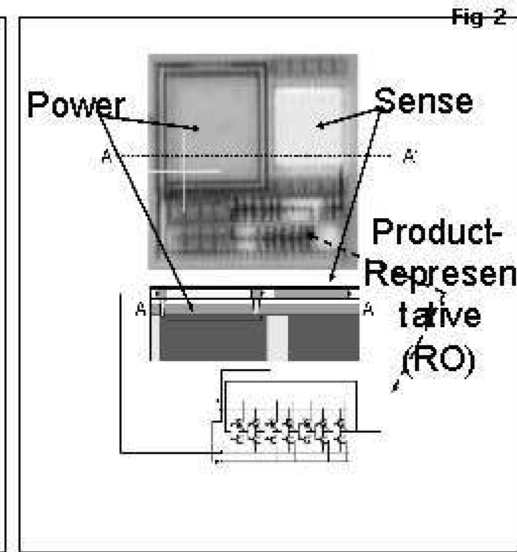


Fig 2

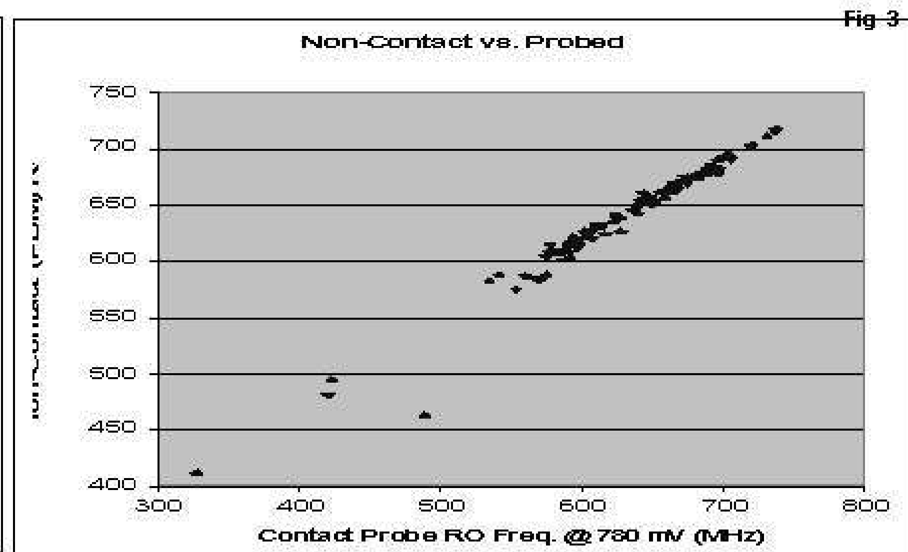
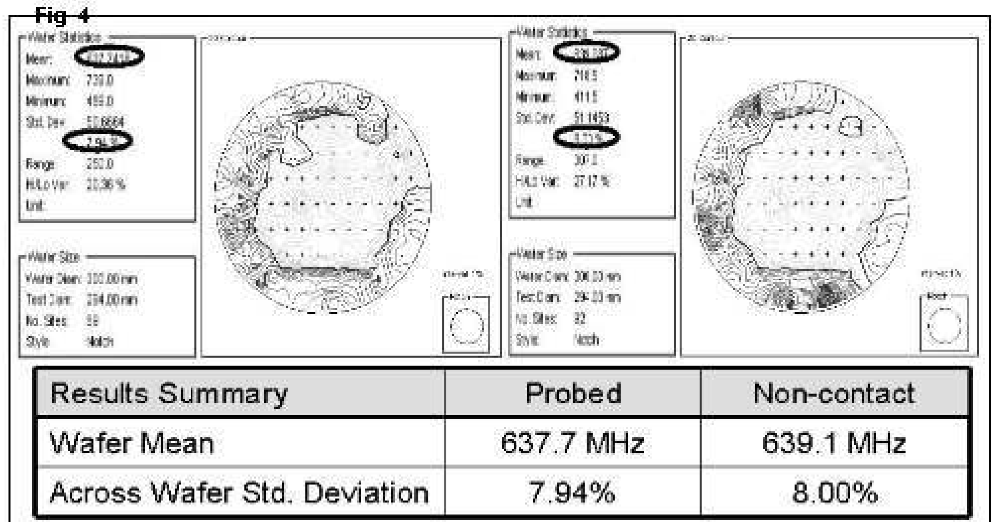
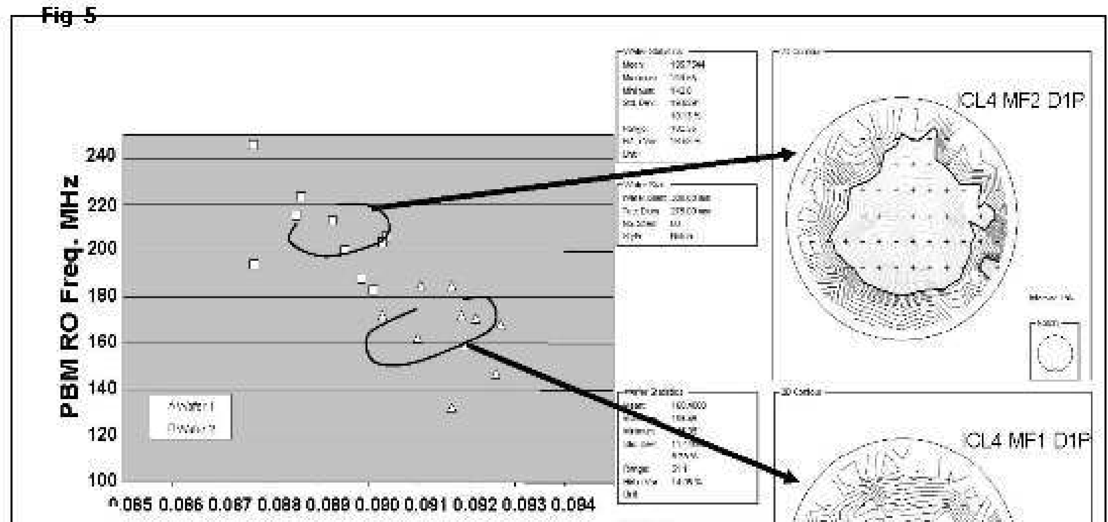


Fig 3



Results Summary	Probed	Non-contact
Wafer Mean	637.7 MHz	639.1 MHz
Across Wafer Std. Deviation	7.94%	8.00%

Fig 4



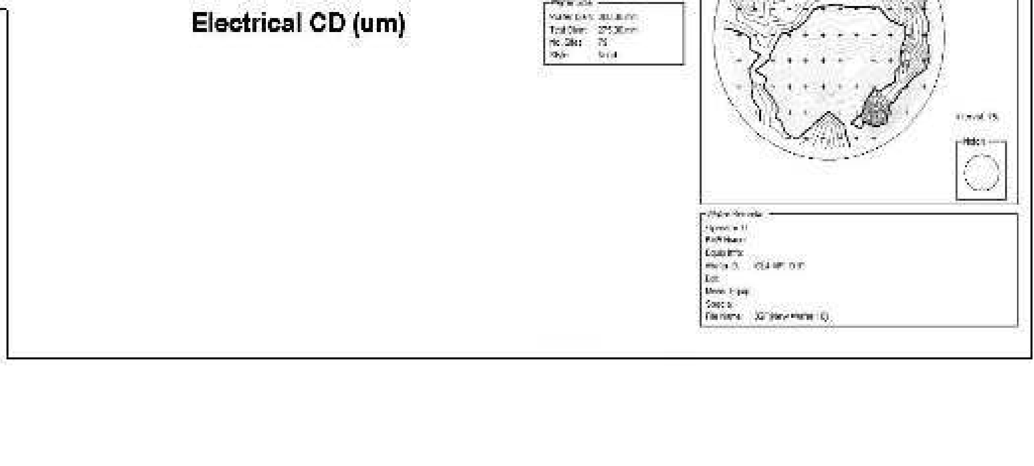


Fig 5

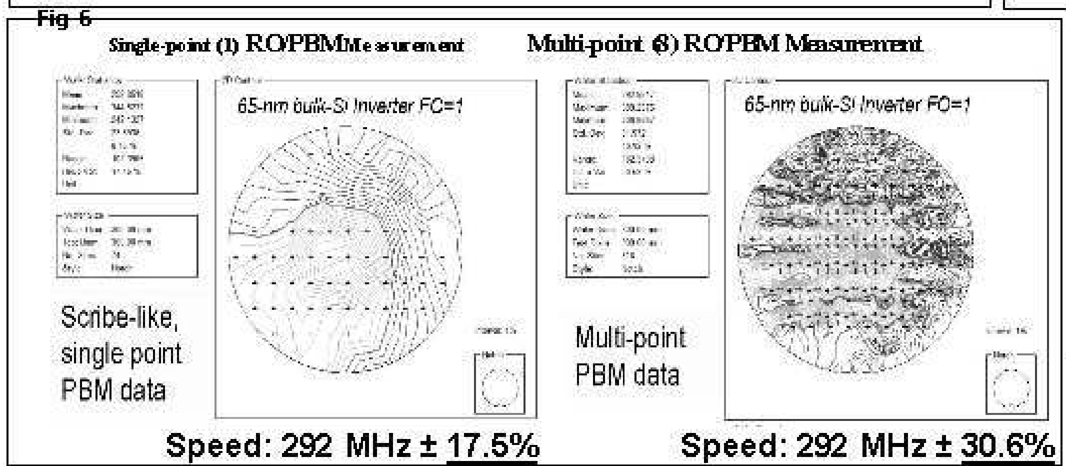


Fig 6