# Non-Contact, Pad-less Measurement Technology and Test Structures for Characterization of Cross-Wafer & In-Die Process-induced Variability

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***Abstract:*** *In-die process induced performance variations are measured on product wafers by non-contact activation of ring oscillator test circuits. Design and characterization of the test circuits and examples of wafer performance data using them are presented.*

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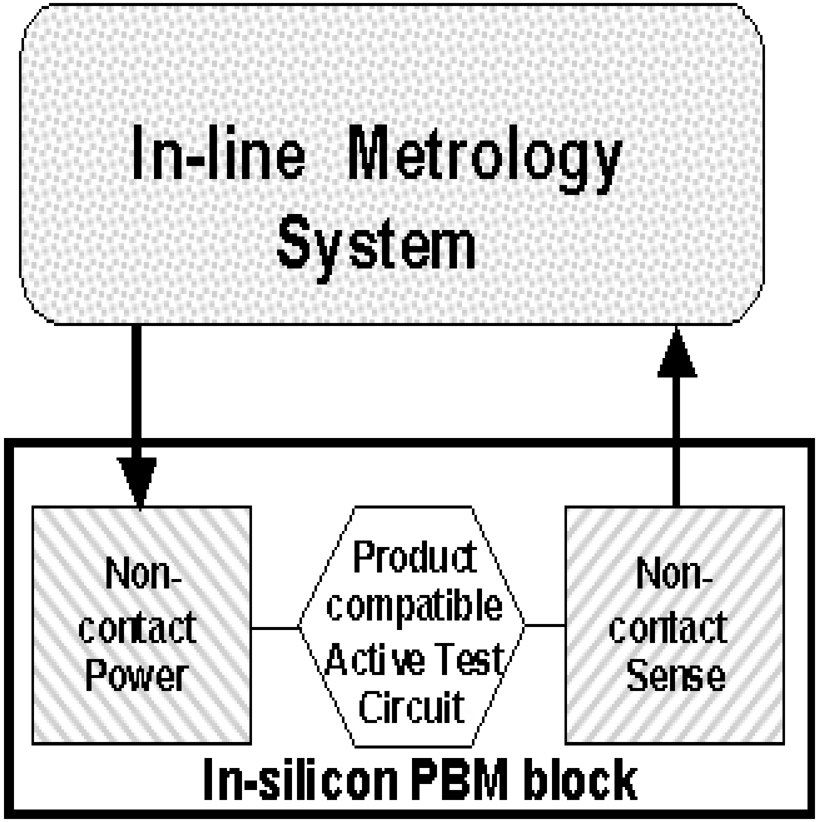
**ST- Crolles:** Jean Galvier , Wim Doedel*, Bertrand Borot, Maxime, Gatefait, Pascal Gouraud, and Patricia Gros
**tau-Metrix :** Gloria Johnson

** NXP assignee to Crolles2 Alliance, currently at EM Microelectronic-Marin SA, Switzerland*

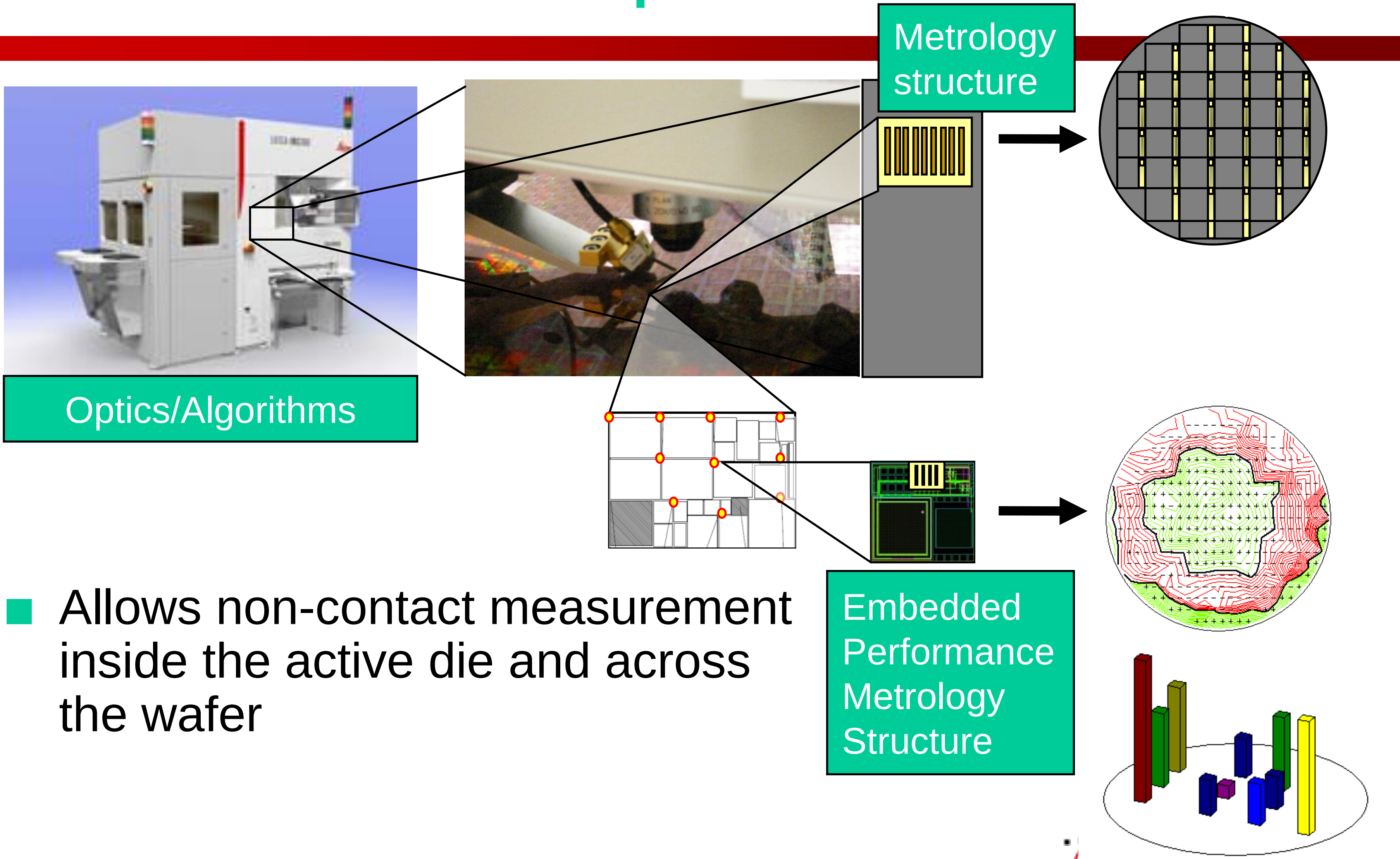
# PBM *Technology Elements*

## *On and Off Silicon*

- **Automated in-line system**
  - Wafer handler & data interface
  - Non-contact power delivery
  - Non-contact signal pickup
- **Product-representative on-wafer targets**
  - Power conversion
  - Active test circuits
  - Signal output



# PBM Couples Metrology and Performance Impact



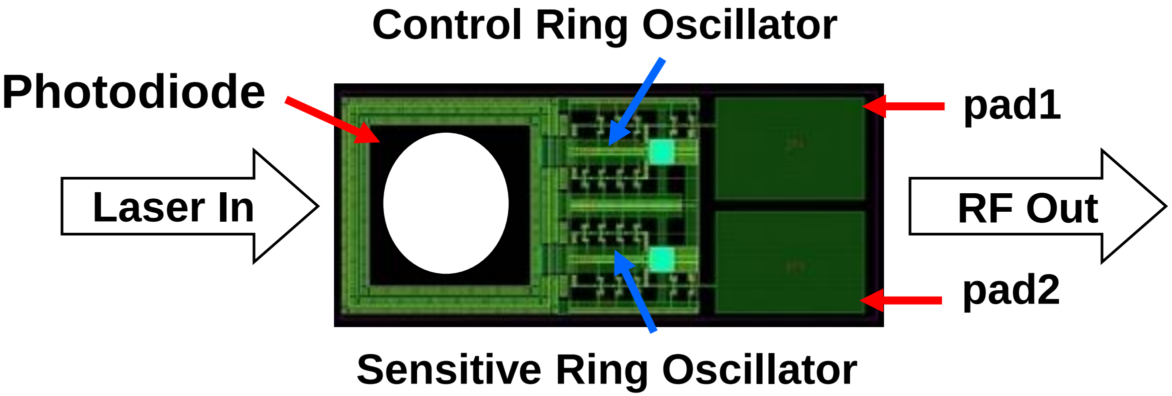
Metrology structure

Optics/Algorithms

Embedded Performance Metrology Structure

- Allows non-contact measurement inside the active die and across the wafer

# PBM:
## *On-silicon Test Structure Design*



**Control Ring Oscillator**

**Photodiode**

**Laser In**

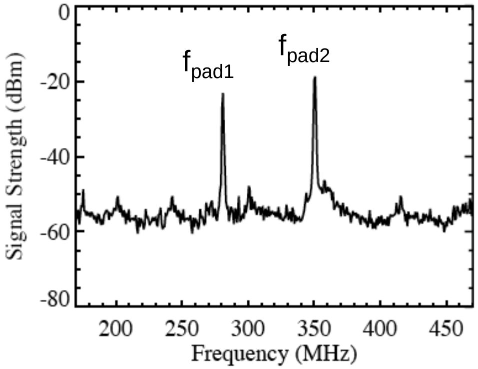
**pad1**

**RF Out**

**pad2**

**Sensitive Ring Oscillator**

**Spectrum Analyzer**

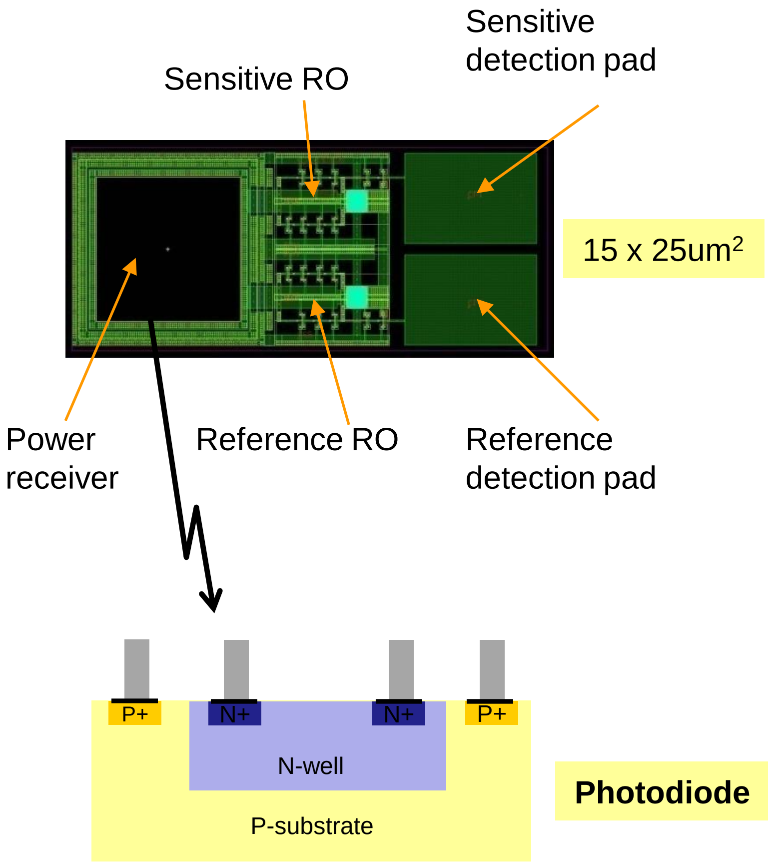


- Small size: ~ 10 by 20 μm, can be placed in scribe or within product
- Autonomous design
  - Self powered and independent of surrounding circuitry
  - Uses standard CMOS design with normal process flow
- Differential construct monitors a control and a sensitive circuit
  - Power supply variations common to both Ros
  - Implemented INV, NAND, NOR, and customer-modified SRAM-based ROs

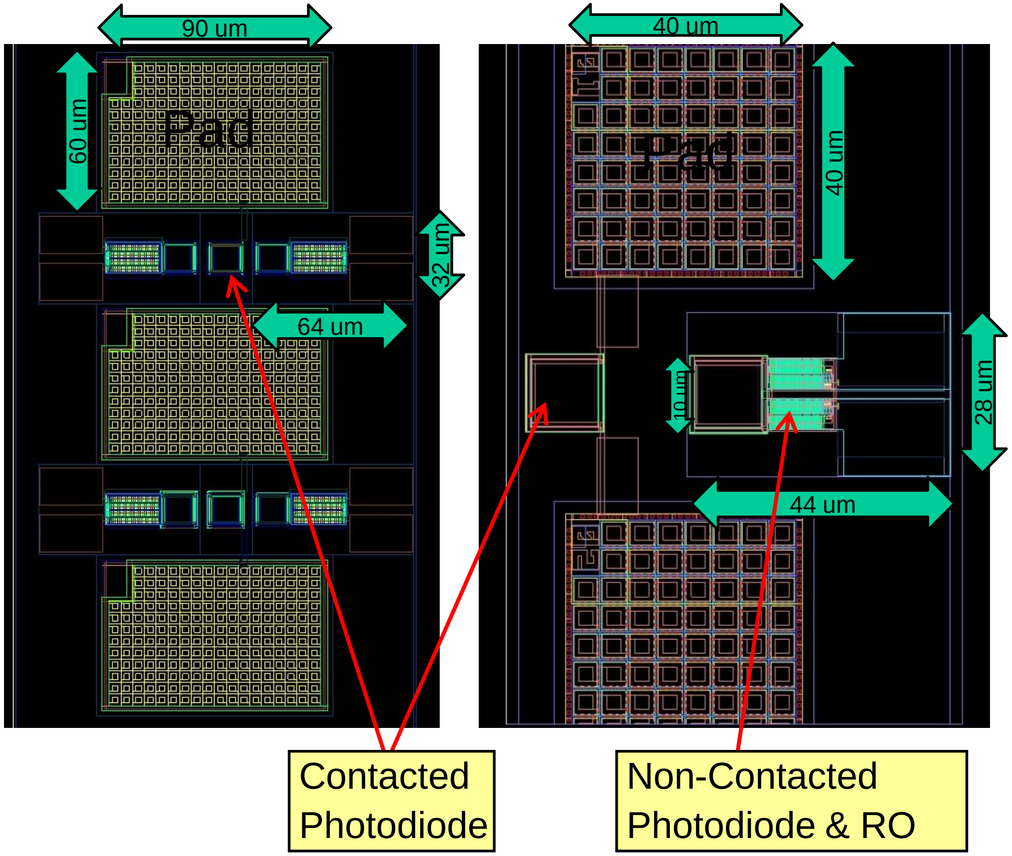
# PBM Basics: Test Block, Photodiode

## Footprint and Layout Examples

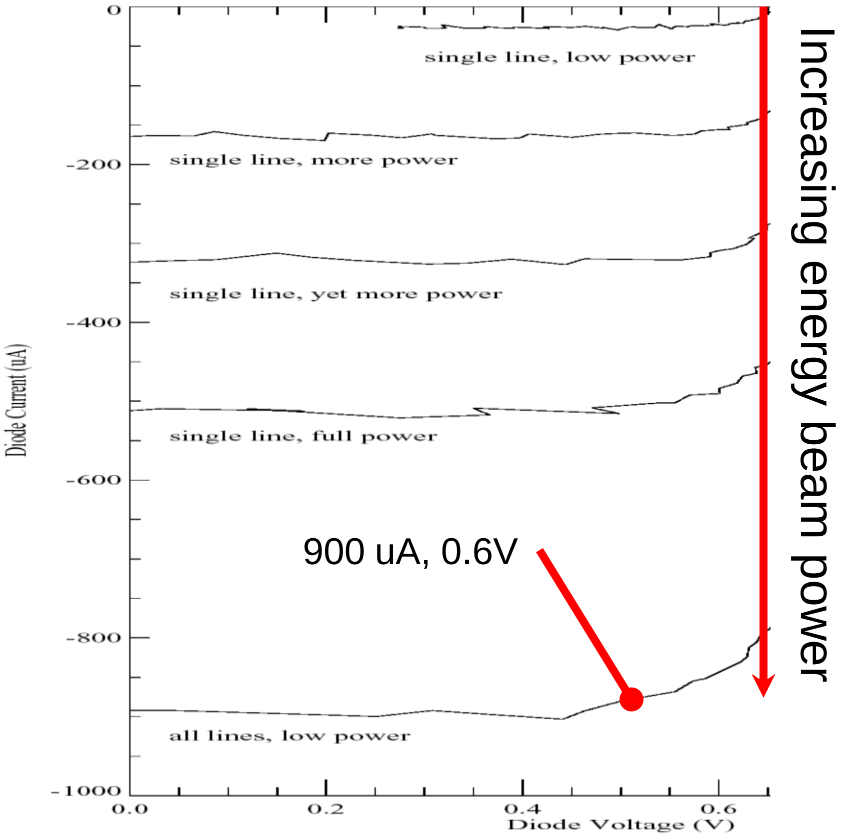
- General PBM Test Block:



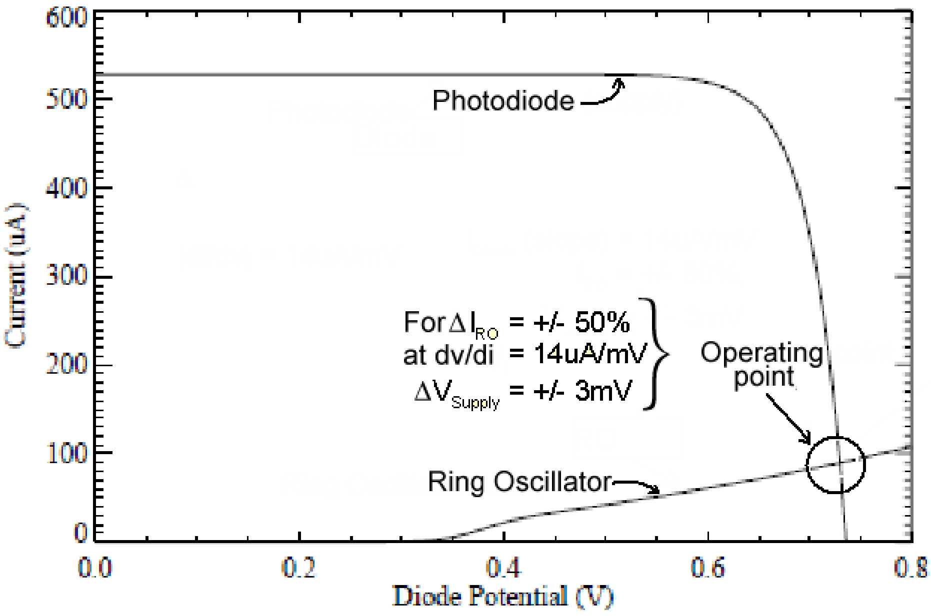
- 45nm PBM Test Block examples:



# Photo-Diode I-V Characteristics



- Increasing the energy beam power increases the generated current



For $\Delta I_{RO}$ = +/- 50%
at dv/di = 14uA/mV
$\Delta V_{Supply}$ = +/- 3mV

- Typical illuminated photodiode I-V with a RO load line

# *Power Supply Characteristics*

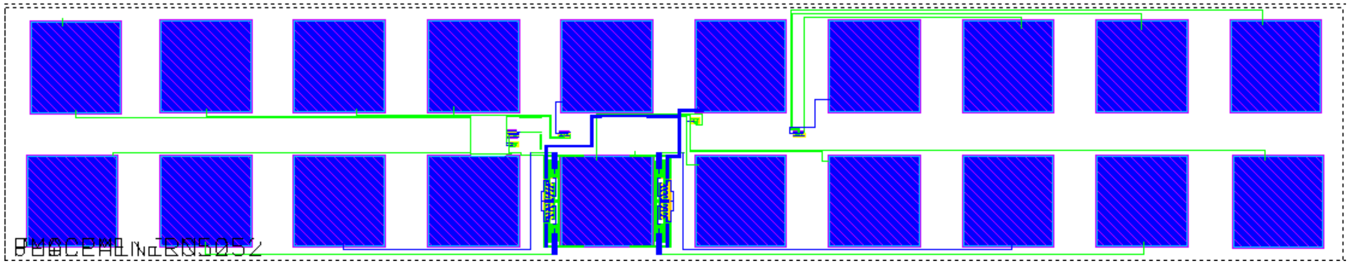
- Across-wafer photodiode performance:
  - Measured 730.2 ± 0.9 mV at M1
  - Measured 717.6 ± 4.6 mV at MF
  - Photodiode voltage regulation is better at M1 ( ~ 1 mV) than at MF (~ 5 mV)
  - Less optical power reaching the photodiode of the MF wafer results in less photovoltaic generation relative to M1 wafer

- Note: The photodiode is also driving a differential RO

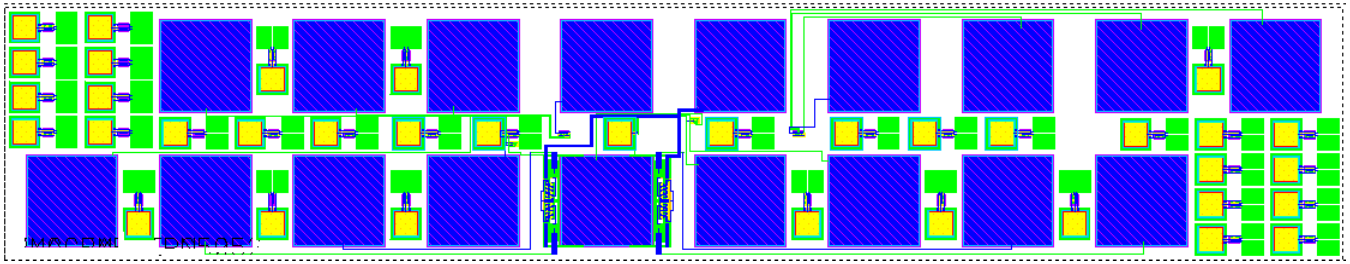
# Non-contact PBM test-structure

*Small Footprint, autonomous, drawn directly from product*
*(65nm Example)*

- ORIGINAL: two RO, PFET & NFET(counters, control logic, and pad buffers)



- PBM + ORIGINAL: two RO, PFET & NFET(counters, control logic, and pad buffers)



- PBM + ORIGINAL: Included original two ROs + 33 additional PBM process and device characterization structures for supplementary learning
- PBM only (no pads): Potential for > 125 PBM test structures within same space

# PBM DUTs:

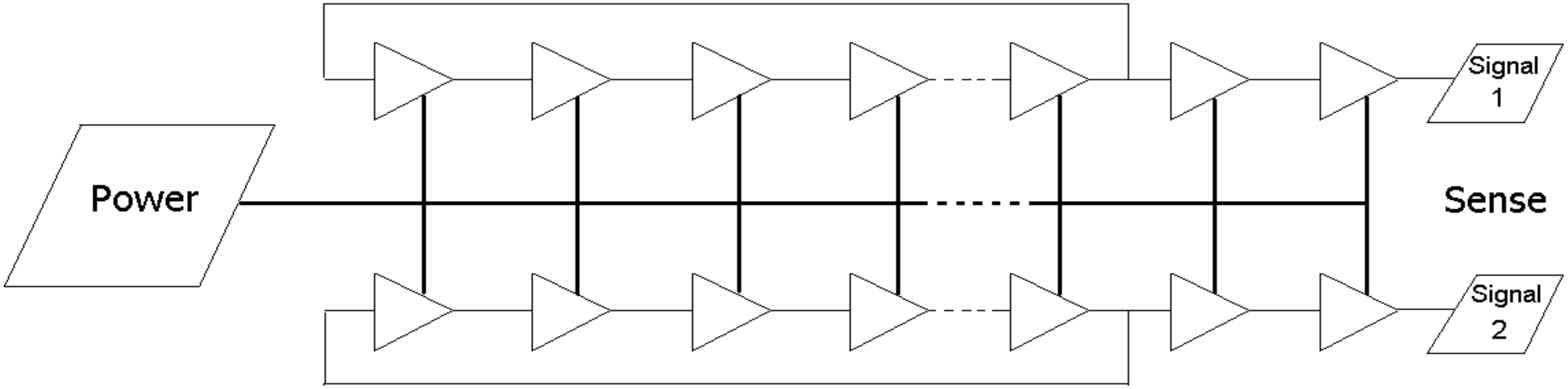
## *Why ring oscillators?*

- Advantages
  - Sub-nanometer sensitivity from micron size structures
  - Power requirements dramatically scaled
  - Standard test circuits with long design and manufacturing history
  - Data familiar to product teams in development and manufacturing
  - Product sensitivity is well represented by product circuits

- But...
  - Often limited to the scribe or final wafer sort or episodic measurements
  - The data comes late, statistics are limited, and there are increasing mismatches with product results

# PBM Ring Oscillator Design

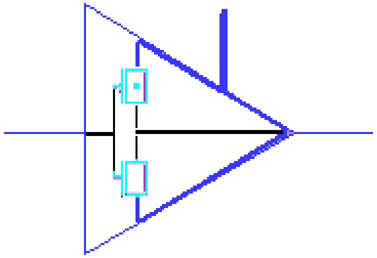
## Differential ROs, Common Power Source



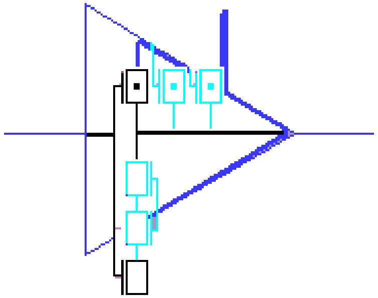
- Cancels voltage variation sensitivity
- Allow discrimination of device or process sensitivities
- Stages with different circuit types, layout geometries, and loadings have different sensitivities to process variation
- Separation and device size vary mismatch and discriminate local/random from systematic process variation

# Ring Oscillator Sensitivities

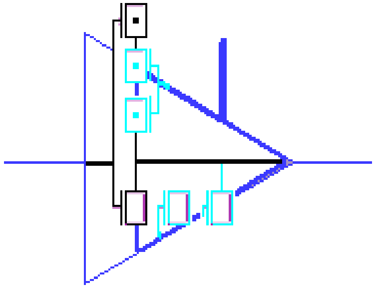
## Inverter Block Designs



INVerter
- switching delay
- sensitive to Leff

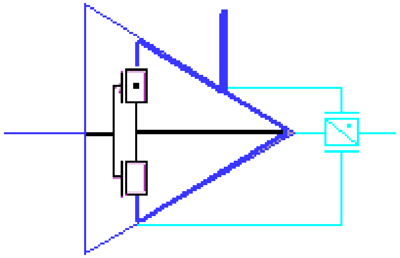


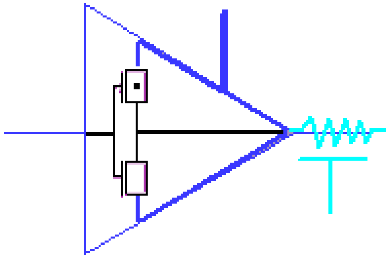
NFET
drive



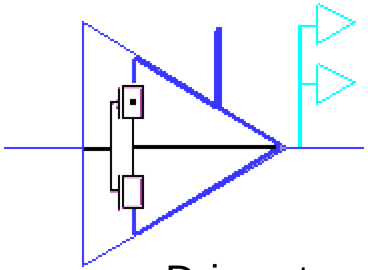
PFET
drive

Threshold
voltage



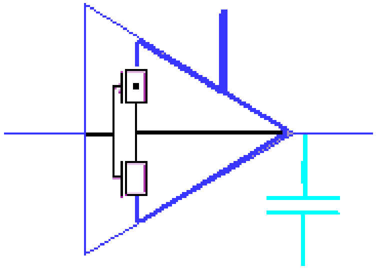


Interconnect
delay



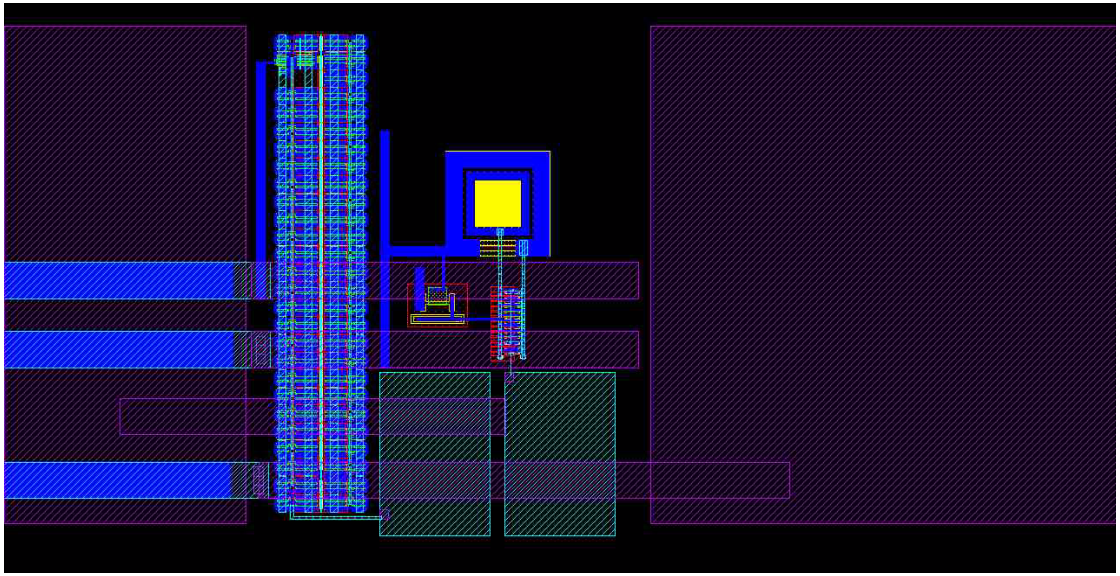
Drive strength
Gate capacitance

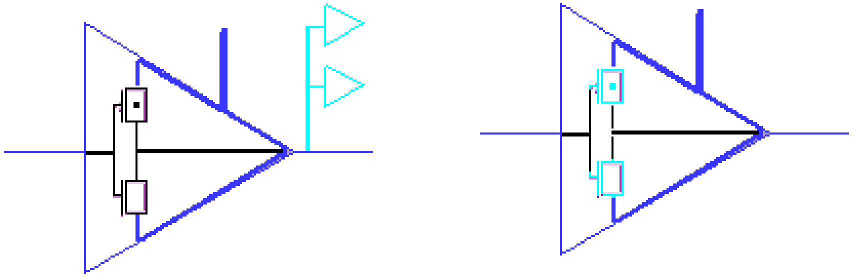
Interconnect,
Gate or other
Capacitance



# PBM RO Design

## Product-Representative RO

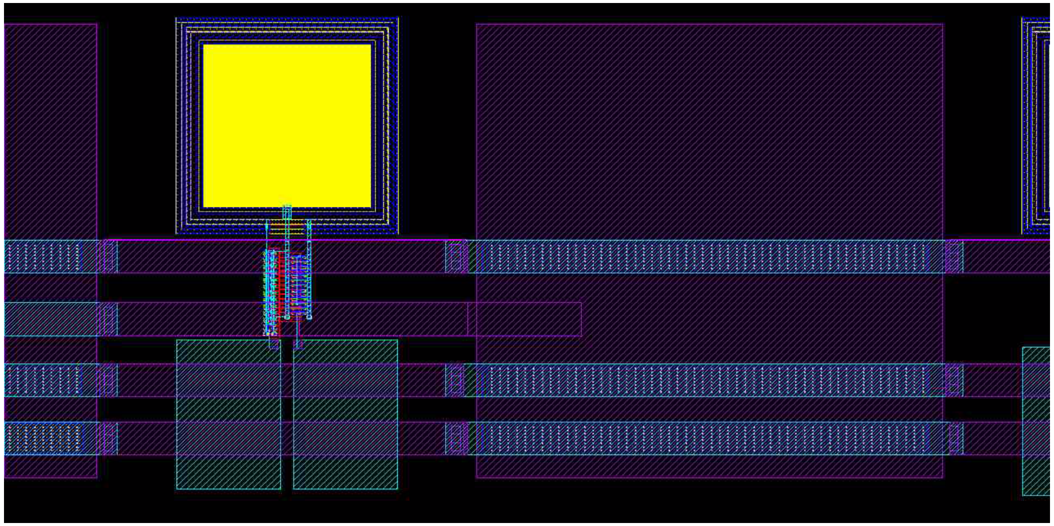


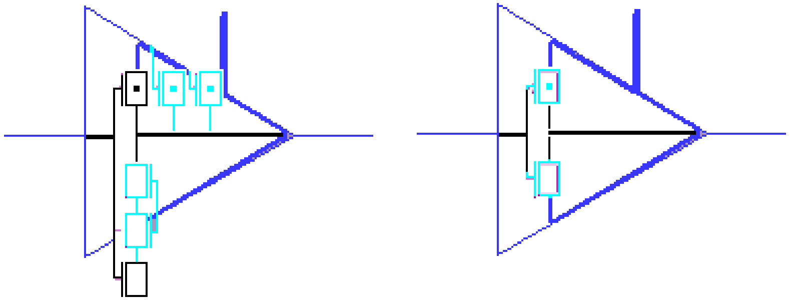


- INV-FO4/INV-FO1
- 5um photo-diode
- Repeat w/3 Tx widths (similar layouts)
- Used for final wafer test performance and power stability evaluation

# PBM RO Design

## NMOSFET Drive Current Sensitivity



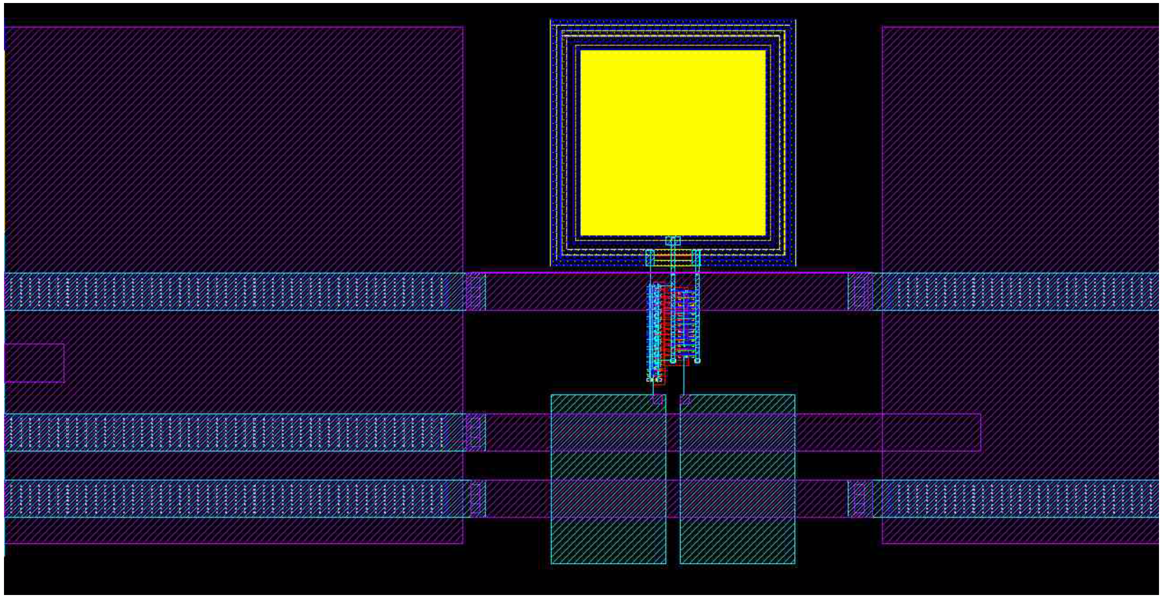


- Scribe RO
- NAND3-FO1/INV-FO1
- 20um photo-diode
- Repeated w/5um diode

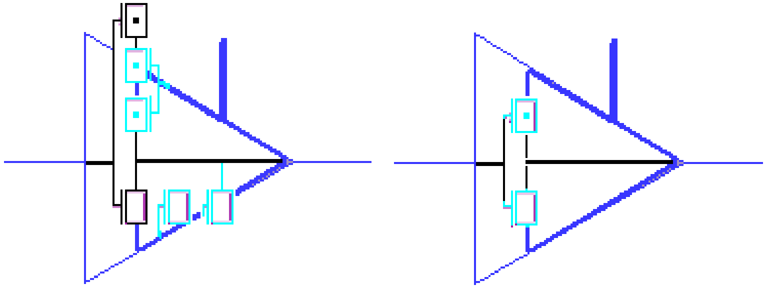
- Used for drive current and power conversion evaluation

# PBM RO Design

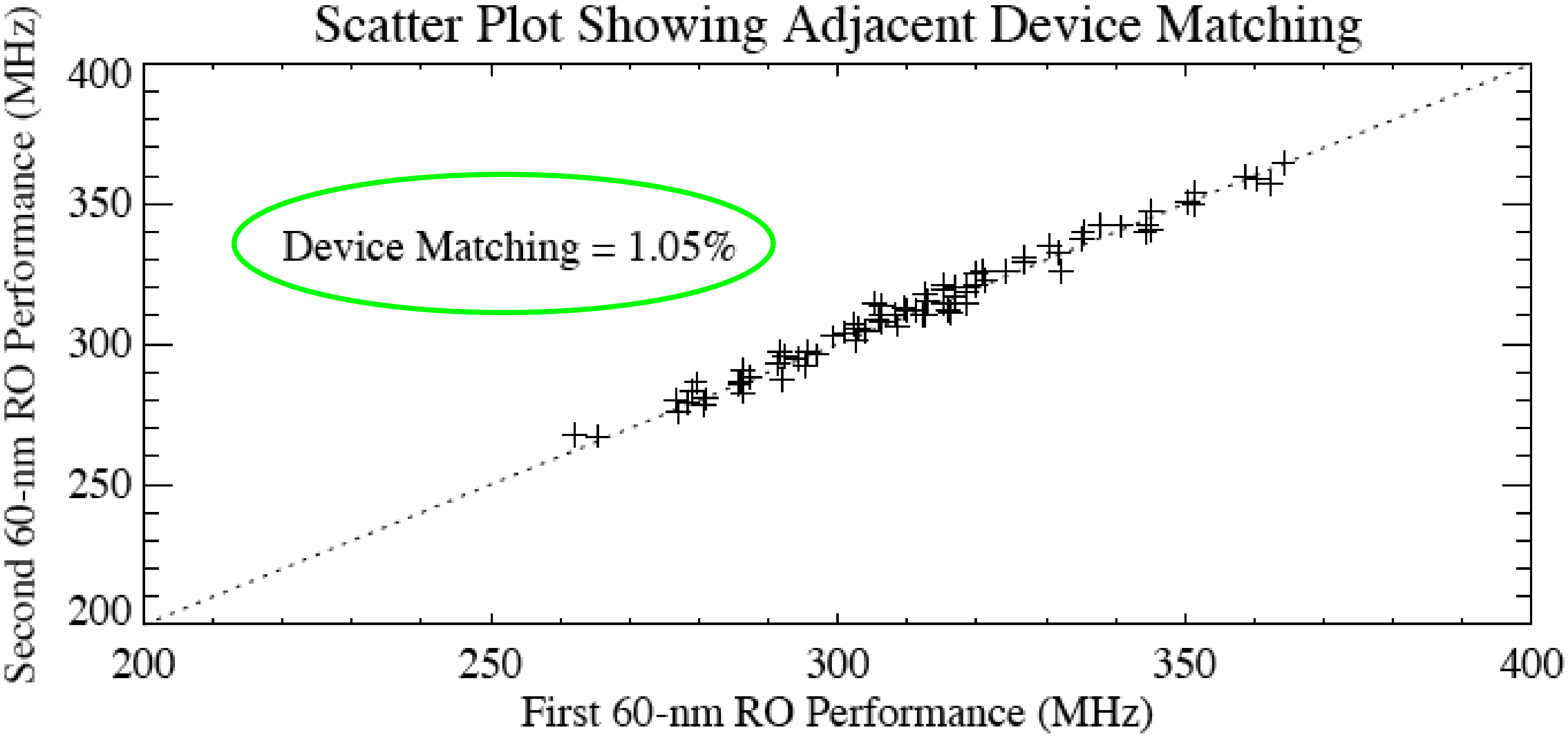
## PMOSFET Drive Current Sensitivity



- Scribe RO
- NOR3-FO1/INV-FO1
- 20um photo-diode
- Repeated w/5um diode
- Used for PFET drive current and power conversion evaluation

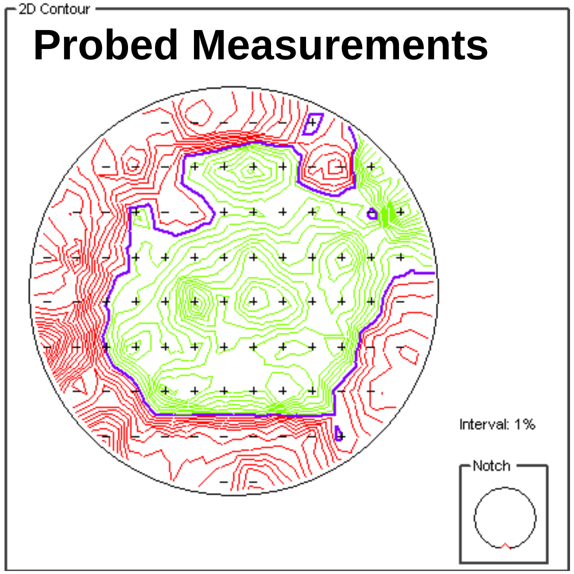


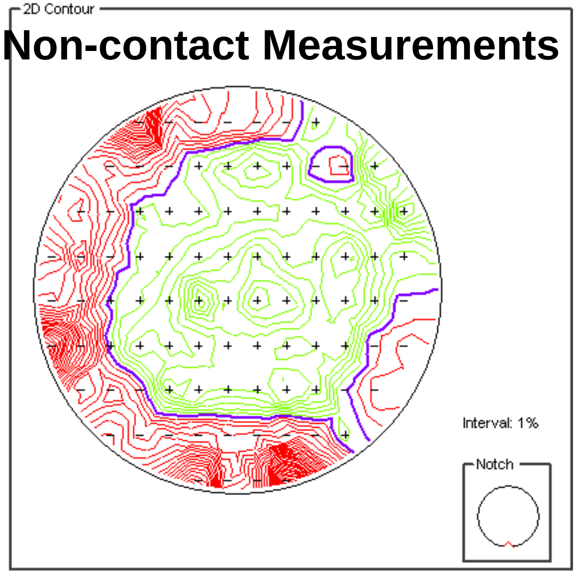
# "Nulling" Differential Test Structure:
## Good Correlation of  Differential RO Results



# PBM Non-Contact vs Probed

## *45nm SOI, Wafer Level Results*


**Probed Measurements**

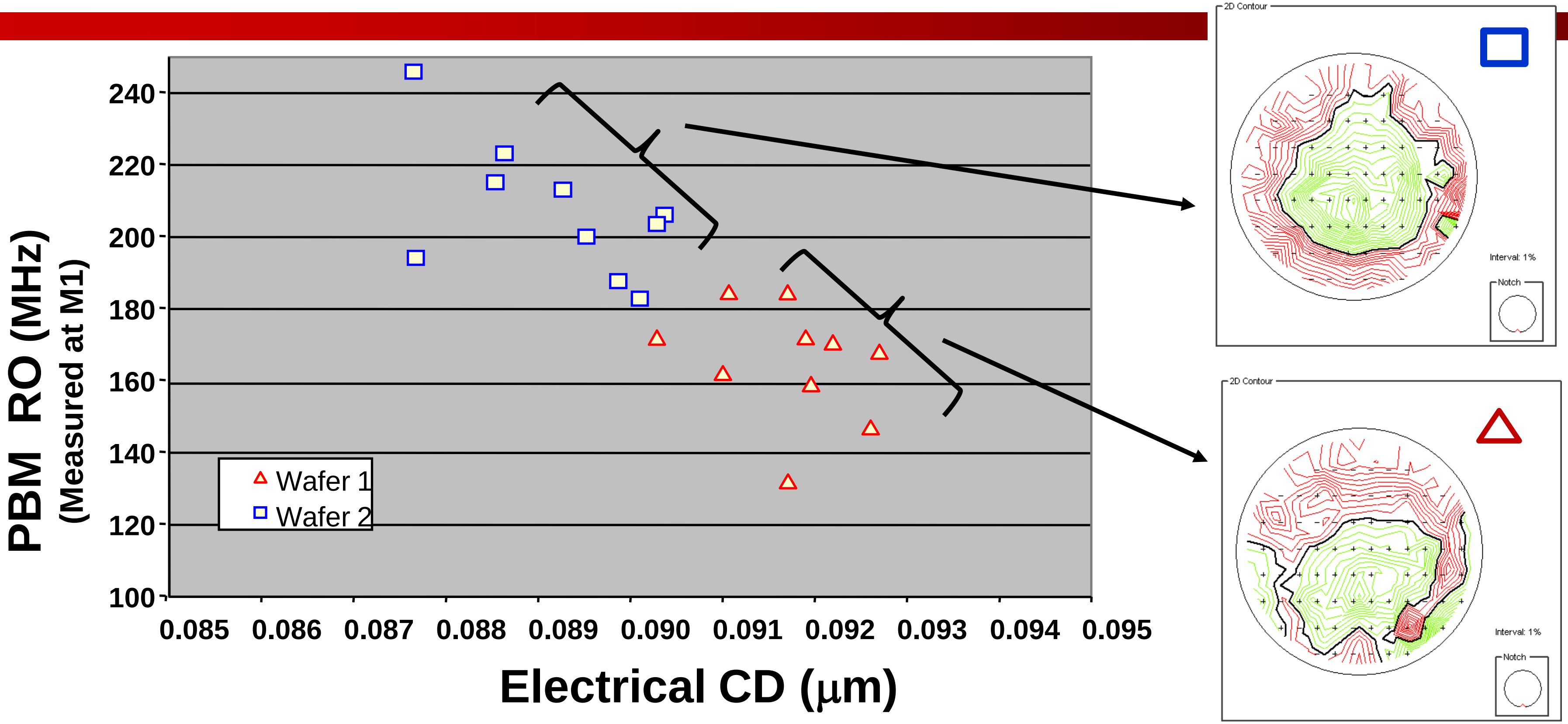

**Non-contact Measurements**

| Results Summary | Probed | Non-contact |
|---|---|---|
| Wafer Mean | 637.7 MHz | 639.1 MHz |
| Across Wafer Std. Deviation | 7.94% | 8.00% |

- Excellent agreement between the wafer mean and distribution, as well as the spatial behavior

# PBM Correlation to eCD Metrology

## *90nm bulk-Si*



- **In-die mapping reveals process fingerprint and identified slower wafer, 15% decrease in speed**

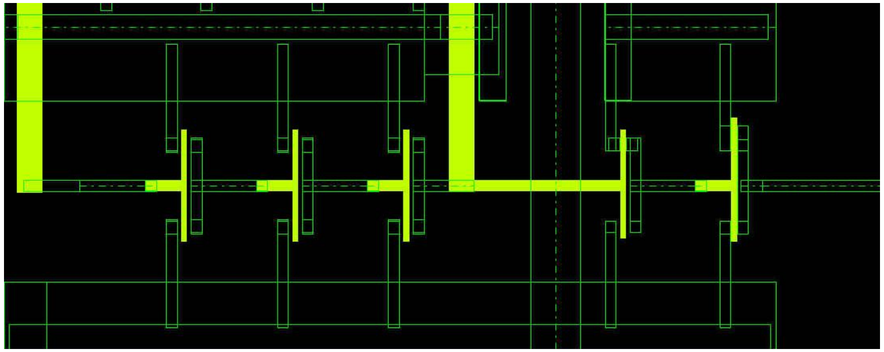
*Source*: Presented at SPIE Advanced Lithography 2006 (San Jose, CA)

# Optical Lithography Proximity Effect:

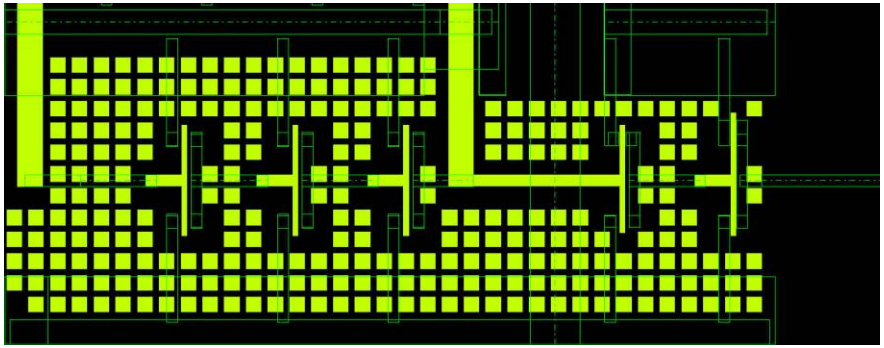
## *Poly Pattern Density Variation*

- Wafer Information:
  - 90nm bulk process
  - Minimum L (100nm) design
  - Built two identical Ros
    - First RO has low poly pattern factor
    - Second RO has high poly pattern factor

Basic Ring Oscillator

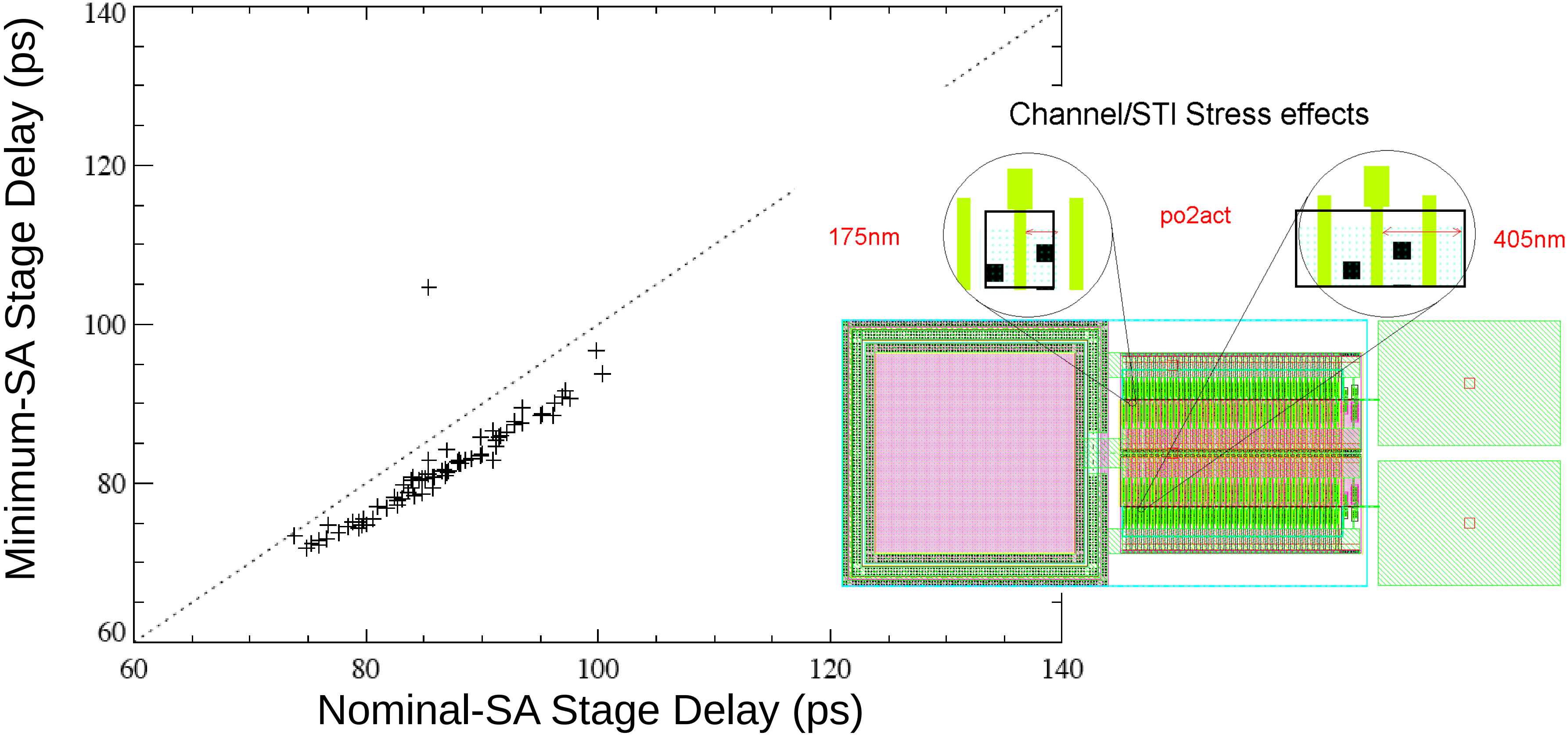


Ring Oscillator with Poly Fill



4.6% slower with added poly

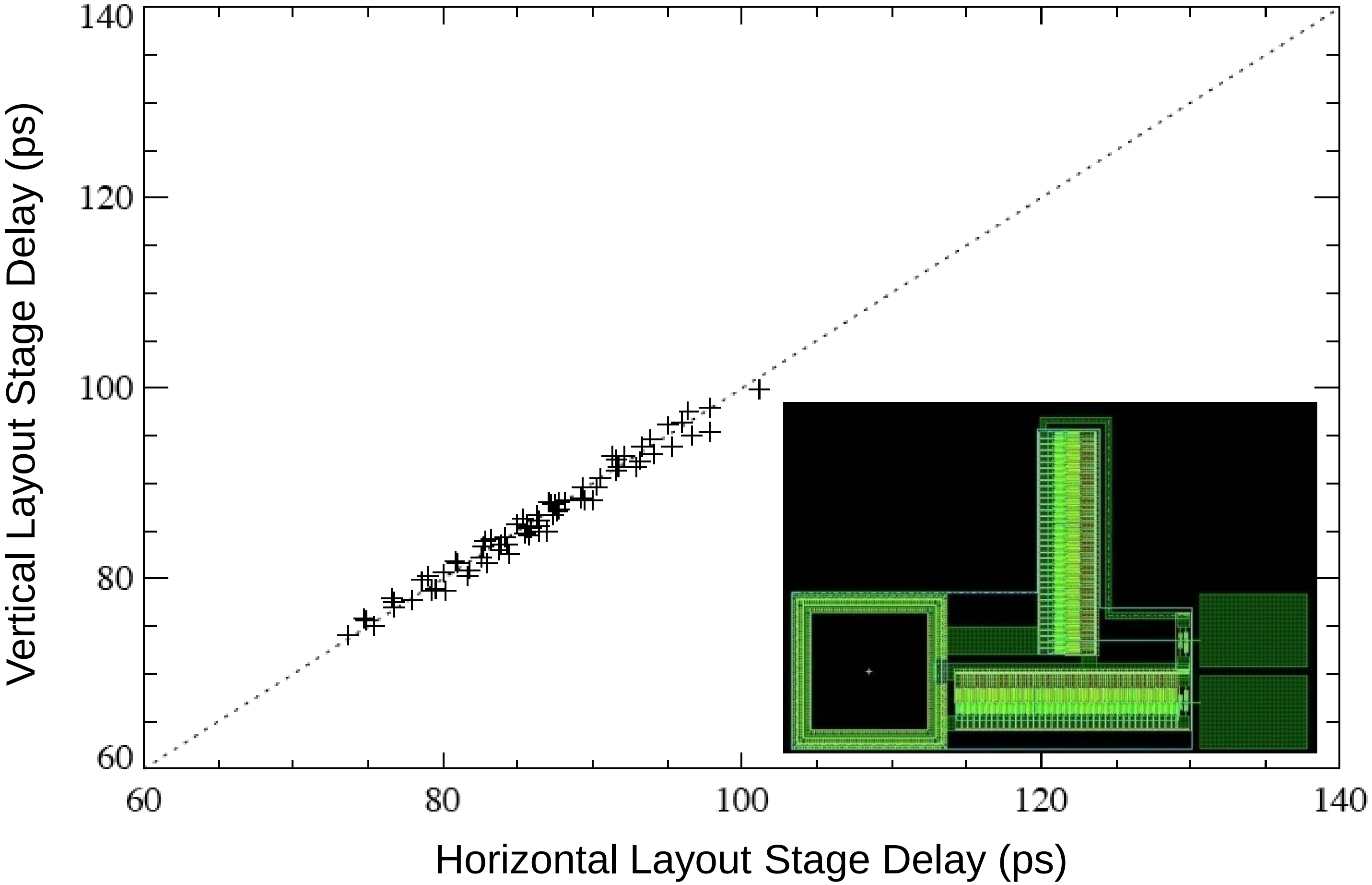
# PBM Poly-to-Active Overlay Variations



- Minimum active space layout devices are ~ 10% faster

# Lithography Orientation Effects

## X vs. Y Layout Effects (65nm bulk-Si)



- Little or no poly orientation effects observed

# PBM Analysis: *A Case Study**

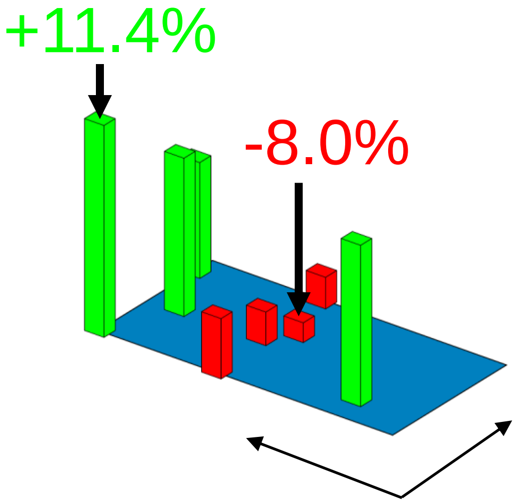
- Early vs. Improved 65-nm bulk-Si results
- Three-wafer process split:
    - Nominal wafer
    - Gate Poly Etch Trim Experiment
    - Gate Poly Exposure Experiment

- ***Summary: Across-wafer $L_{EFF}$ variations dominate physical CD variations***

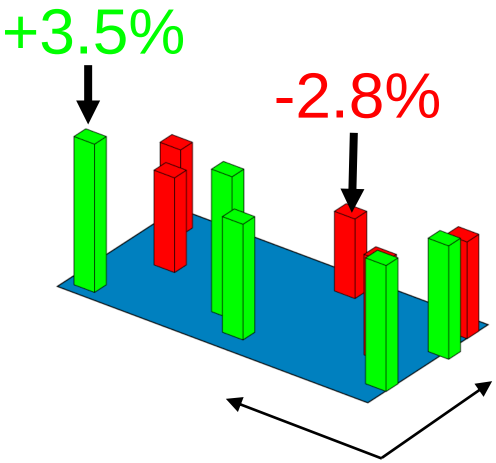
***** *Source*: Presented at SEMI 2008 (Chiba, Japan ) & SPIE Advanced Lithography 2009 (San Jose, CA)

# Early vs. Improved Process

*65nm bulk-Si, Sensitive RO (L = 60-nm), All Reticles Averaged*



Early 65-nm process
(~20% in-die variation)

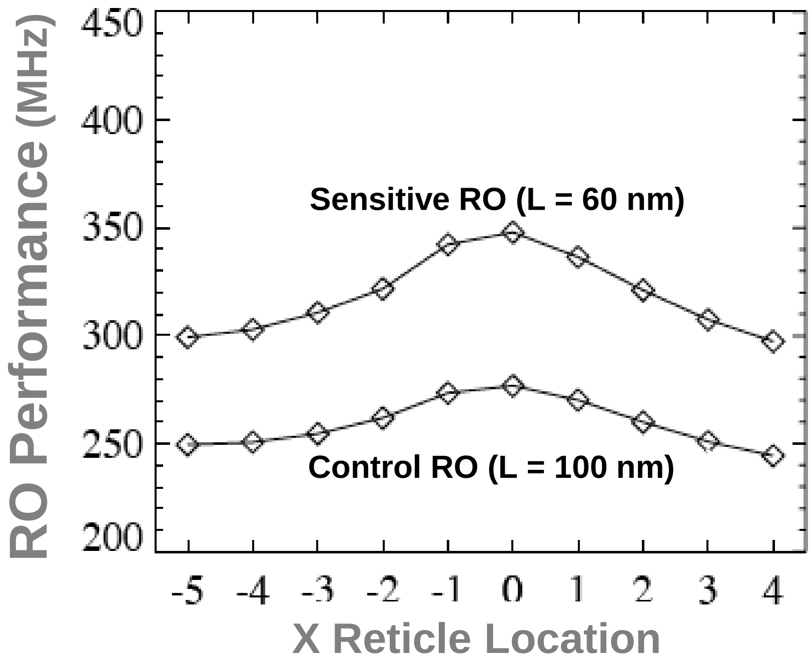


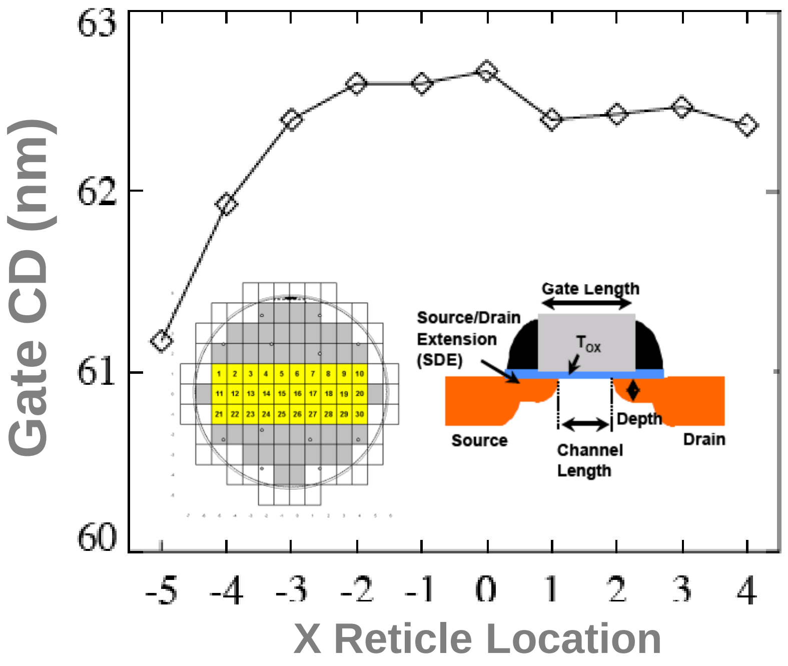
Improved 65-nm process
(~6% in-die variation)

- Across-Die Variation Improvement
- Shorten yield ramp time using in-die performance data

# Nominal (Optimized) Process

*Measured RO Performance vs. Measured Gate CD*

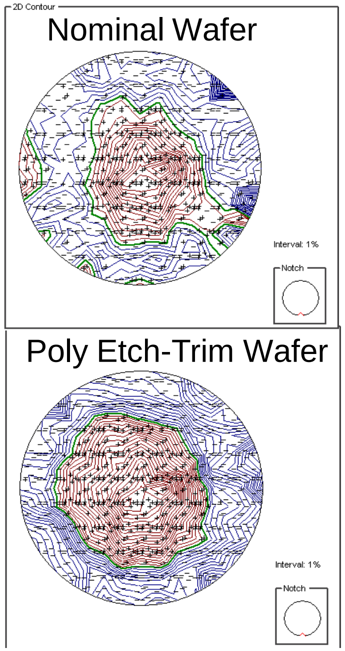


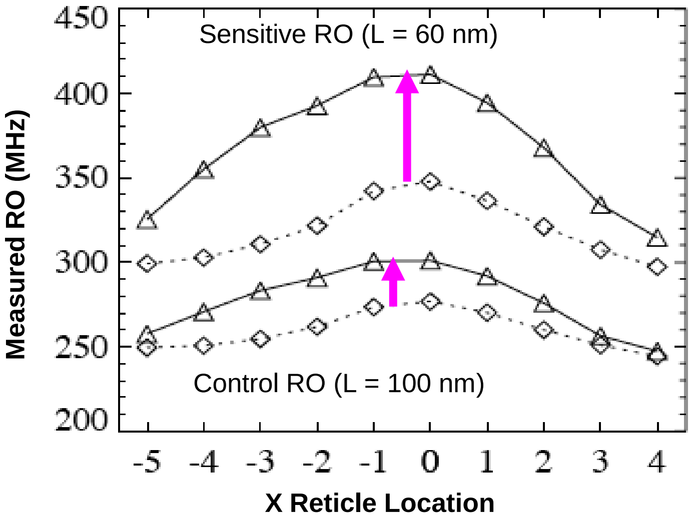


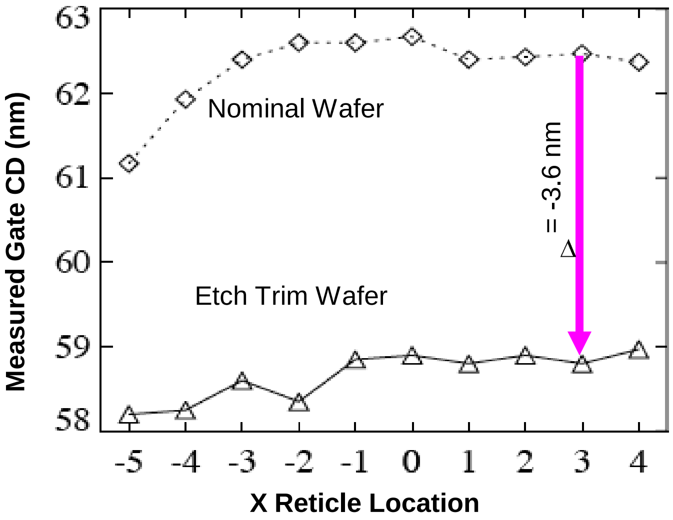
- Wafer CD Poly Measurements - Target Poly = 64 nm
- 3.5% CD spread **cannot** explain 30% RO performance spread
- Measured RO performance ($L_{EFF}$) is not correlated with gate CD

# Gate Poly Etch-Trim

## *RO Performance Sensitivity: PBM » Physical CD*



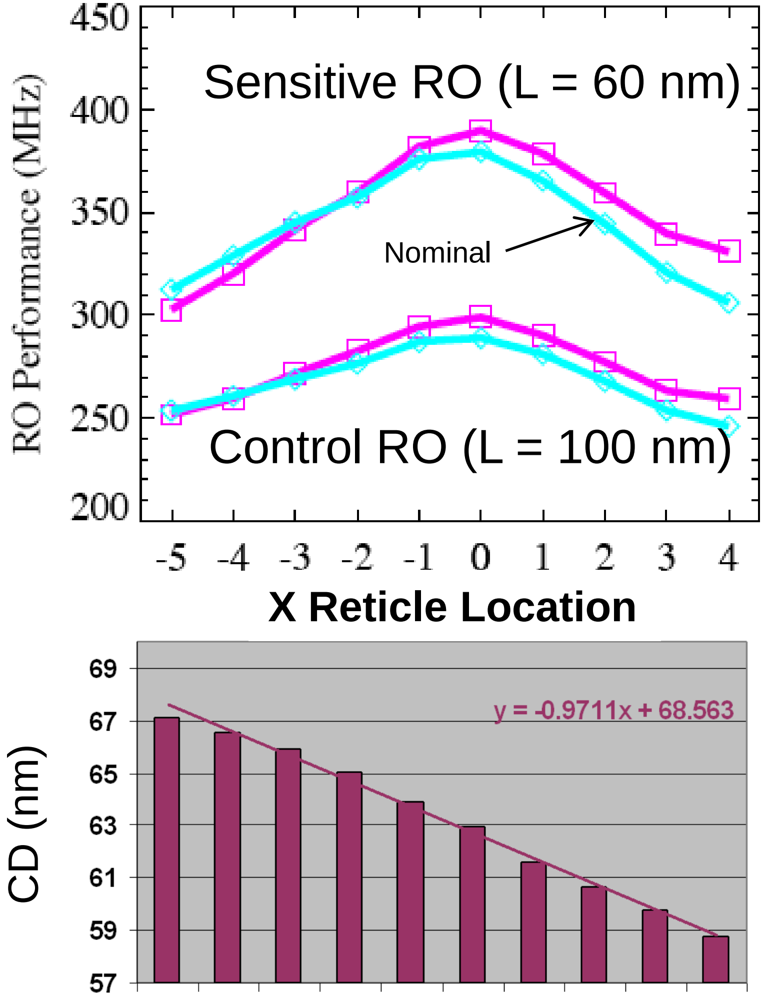




- Nominal Wafer, RO (L = 60nm), Ave. Freq.= 308.3 MHz, 1s =18.1 MHz
- -4nm Poly Etch-Trim Wafer, RO (L = 60nm), Ave Freq. = 338.8 MHz, 1s= 39.6 MHz
- Speed increased < 10%, performance variation increased > 100%
- Etch trim affects short-channel device more than long-channel device

# Gate Poly Striped Dose-Exposure

## *RO Performance Sensitivity: PBM » Physical CD*



- Striped Exposure Wafer
  - Target Poly CD Variation = -1 nm/stripe
  - CD affect more pronounced on short-channel RO
  - Average Freq. (L=60nm) = 329.2 MHz, 1$\sigma$ = 32.1 MHz
  - Nominal wafer : Average Freq. (L=60nm) = 308.3 MHz, 1$\sigma$ = 18.1 MHz
- Across-wafer $L_{EFF}$ variations dominate exposure-induced CD variations

# Summary

- These results demonstrate an innovative non-contact, performance-based metrology technique (PBM)
- The technique can be applied during manufacturing to directly measure in-die, cross wafer, and cross-line variability
- Early process learning can be carried into volume production and final wafer yield becomes visible from first connectivity onward, accelerating yield ramp, maintaining high productivity, and improving efficiency