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Improving the Power-Performance of Multicore Processors Through Optimization of Lithography and Thermal Processing

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ABSTRACT

It is generally assumed that achieving a narrow distribution of physical gate length (Lpoly) for the poly conductor layer helps improve power performance metrics of modern integrated circuits. However, in advanced 90 nm technologies, there are other drivers of chip performance. In this paper we show that a global optimization of all variables is necessary to achieve the optimum performance at the lowest leakage. We will also describe how systematic physical gate-length variation can improve core matching in multicore designs.

Keywords: ACLV, CD control, PSRO delay, Cov, Leff, Variation

1. INTRODUCTION

The 90 nm node technology developed for high-performance processors had electrical gate length (Leff) control as a critical goal from the initial development stages.[1,2] By reducing the variation of Leff, power-performance metrics were continually improved as the products matured in manufacturing. It is important to note the difference between Leff and Lpoly which is the physical gate-length. Although they are related, Leff is determined by more than the Lpoly alone. Too often it is assumed that decreasing Lpoly variation will lead to micro-processors with less leakage at high frequency. Indeed, we and others have published on the importance of decreasing variability of the physical gate length.[3,4] Many of the important topics discussed annually at the SPIE International Symposium on Microlithography such as OPC,[5] improved exposure tools and masks, increased process window, DFM, etc. are directly applicable to decreasing Lpoly variation. This paper demonstrates that decreasing Lpoly variation does not necessarily decrease device speed variation as measured by product sensitive ring oscillators (PSRO). It will demonstrate that only by decreasing Leff variation can PSRO variation be decreased. Learning how to control and minimize Leff variation is the key to improving performance, while decreasing unwanted leakage, of future generations of integrated circuits.

2. RESULTS AND DISCUSSION

2.1 Influence of physical gate length on PSRO variability

An aggressive across chip line-width variation (ACLV) value was targeted for the poly conductor layer critical dimension (CD) after etch for the 90 nm node. This goal was achieved through significant focus on every aspect of CD control. Optical proximity correction (OPC) models were created to correct through pitch variation. Site to site variation was driven lower by improving mask processes, exposure tools, lithographic process window, and etch process (Figure 1). Topography and orientation effects were also reduced. With a gate process capable of achieving less than 2.4 nm 3-sigma variation (Figure 1B), three different systematic CD signatures were printed across a field that had 24 PSROs using across field dose compensation.[6] Figure 2 shows the resulting CD profiles across the scan of the field after etch. The first “frowned” and had CDs ~1.5 nm smaller at the start and end of the scan than in the center of the scan, the second was flat and the third “smiled” and had CDs ~3 nm larger at the start and end of the scan than in the center of the scan. If Lpoly variation were the sole driver of PSRO variation then it would be expected that the fields printed with the flat CD signature would have the least PSRO variation. This is not what was found. Going from a frowning CD signature to the flat systematic CD signature across the scan did reduce the PSRO variation. However, the flat CD signature across the scan did not lead to a flat PSRO delay signature across the field (Figure 3).[7] Instead the flat CD

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signature still resulted in the PSROs at the start and end of the scan switching faster than those in the center of scan. In fact, even when the smile CD signature was used, the PSROs at the start and end of the scan switched faster than those in the center of scan. While all three systematic CD signatures resulted in a PSRO signature having faster PSROs at the start and end of the scan, going from the frowning to smiling CD signature reduced the systematic portion of the PSRO delay signature by 45% (Figure 3).

Figure 4 shows the relationship between the PSRO delay and final CD for two different CD signatures. The frowning CD signature led to a positive slope, i.e. larger CDs led to slower PSROs (longer delay). However, the plot using the smiling CD signature had a negative slope; that is the fastest PSROs had largest CD. This result indicates that the PSRO delay variation is driven by components in addition to the physical CD of the gate. Specifically, to achieve the best power-performance tradeoff, dose compensation was used to create an optimal physical CD profile across the field. At constant leakage (IDDQ) the “smiling CD” signature decreased the PSRO delay 6% (Figure 5). Yield of all good chips doubled. These large improvements demonstrate the potential of dose compensation to create systematic CD signatures to compensate for other processes that have across field systematics.

2.2 Relationship between Lpoly and Leff

Increasing the physical gate-length variation across the field and achieving improved micro-processor performance clearly challenges the widely held belief that decreasing the variation of the physical gate length will always be beneficial. Why is this conventional belief no longer true? The answer is that it was never true. As Verhaegan et al. have stated the important gate-length to control is not the physical dimension but the effective electrical gate length (Leff).[8] The approach that they described, using dose compensation to try to decrease PSRO delay variation across the wafer, is analogous to what we have demonstrated across the field. Indeed, Verhaegan et al. demonstrated a case in which in order to decrease the across wafer CD variation after etch and PSRO variation an increase in across wafer CD variability measured in the resist image was required. Where the paper by Verhaegan et al. focused on improving across wafer PSRO uniformity this paper is focusing on within field and within chip PSRO uniformity.

The fact that increasing the systematic variation of the physical gate length (after etch) with the “smile” CD signature across the field decreased the PSRO variation simply means that it is compensating for another parameter that influences Leff. The remainder of this section describes why this occurs in the 90 nm node.

Physical gate-length, overlap capacitance (Cov), dose for the halo implants and other variables are all important in determining Leff. In the 90 nm node, the systematic variable that the systematic CD signatures compensate for is Cov. Cov is affected by the diffusion of the extension implants. This diffusion is directly related to the peak temperature achieved during the rapid thermal anneal process(RTA). In order achieve sharp junction profiles, the industry has progressively implemented shorter anneal times.[9] While the typical anneal time for previous generations lead to thermal diffusion lengths of greater than 20 mm, in the 90 nm node thermal diffusion lengths of 5 mm are typical. For pre-90 nm node generations the 20 mm thermal diffusion length resulted in uniform peak RTA temperature across a 25X25 mm field. However, in the 90 nm node if different areas of a field couple in more energy from the RTA lamp, thermal diffusion may not be sufficient to create uniform peak temperature across the field.

While Cov and Lpoly together determine Leff, we wanted to demonstrate that in some cases, such as that described in section 2.1, Cov variation can be the main driver of Leff variation. To do this, Lpoly and Cov electrically testable macros were placed next to PSROs. Plotting PSRO delay vs. Lpoly no correlation was found (Figure 6A). However, plotting PSRO delay vs. Cov a strong correlation was found where increasing Cov led to shorter PSRO delay (Figure 6B). To further reduce the PSRO delay variation, the RTA process was optimized.[10] By improving the RTA process, the PSRO delay variation across the field was decreased from 9.0% to 3.8% (Figure 7). The optimized process allowed uniform peak temperature to be achieved across the field while providing similar dopant profiles.[11] Along with decreasing the variation, the optimized RTA also removed much of the systematic delay variation across the field.

2.3 Systematic Leff variation affects multicore processors:

The previous two sections have focused on Leff variation that is spatially systematic rather than random. While random variation is detrimental to achieving power-performance metrics, systematic Leff variation can have significant impact on multicore processors. When manufacturing dual-core processors, a new term we introduce called core average Leff delta (CALD) tracks the delta in average Leff between the two cores caused by a systematic Leff signature across the field (Figure 8). A non-zero CALD value will result in cores operating at different speeds and/or leakage. The CALD term is only useful for dual-core processors. With multicore processors, core average Leff variation (CALV) becomes

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important. Of course, ACLV is present no matter how many cores per chip and chips per field exist. However, chip mean variation (CMV) only gets a component from within the reticle field if there is more than one chip per field (Figure 8).

The influence of CALD on the multichip reticle with the chiplet and core layout shown in figure 9 is illustrative. Figure 10 shows the IDDQ delta between the two cores. As the figure shows, core 0 has higher leakage (IDDQ) than core 1 for chiplets A and A’ as the frequency increases above the target. However, for chiplets B and B’ the situation is reversed due to across field systematic Leff variations as were described in sections 2.1 and 2.2. Figure 11 illustrates the physical Lpoly variation across the field. Because of the layout of the chiplets within the field, the smaller Lpoly values are found in core 0 of chiplets A and A’ and core 1 of chiplets B and B’. These smaller Lpoly values correlate in the case of this product to the higher leakage at constant PSRO delay shown in figure 10. By implementing the dose compensation technique described in section 2.1, the frequency of each chiplet can be increased by improving the matching between cores. Specifically, the Leff of the core that has higher leakage can be increased to match both the PSRO delay and leakage of the other core. As shown in Figure 12, after dose compensation the IDDQ delta decreased as the PSRO delay decreased below the nominal target.

2.4 Redefinition of ACLV and how to calculate ACLV when systematic line-width variations are desired:

In section 2.1 we defined ACLV as across chip line-width variation. The previous sections have illustrated that it is critical to understand whether the “line-width” being referred to is the physical gate length or the Leff. When the L in ACLV is Leff, the goal should be to minimize ACLV, both through decreasing the random and across field systematics. However when the L refers to the physical gate length the goal should be to reduce the random residuals while delivering the systematic across field signature that is optimal for decreasing Leff variation. Specifically, when “L” refers to physical gate length, ACLV needs to be redefined as the 3-sigma variation of difference between desired CD value at given point within the field and that actually achieved. If the desired physical value is constant across the field the ACLV calculation will simply be the 3 sigma value of CD measurements made.

3. CONCLUSIONS

To meet power-performance targets all sources of Leff variation need to be minimized. In addition to physical CD control, all other processes that influence Leff control such as junction-anneal and spacer processes must be optimized. Developing independent patterning, junction-anneal and spacer processes that each result in minimal variation across a field is preferred. However, as devices become more complex and processors migrate to multi-core designs, CD compensation for other systematic variations can be used to achieve the optimal power-performance tradeoff.

REFERENCES

1. H. S. Yang et al., IEDM Tech. Dig., Dec 2004, p. 1075
2. A. Mahorowala et al., Proc. SPIE Int. Soc. Opt. Eng. 6156, 61560M (2006)
3. A. H. Gabor et al., Proc. SPIE Int. Soc. Opt. Eng. 4346, 259 (2001)
4. A. H. Gabor, S. D. Halle, and C. Kallingal, Proc. SPIE Int. Soc. Opt. Eng. 5753, 699 (2005)
5. L. Hong, T. Brist, P. LaCour, J. Sturtevant, M. Niehoff, and P. Niedermaier, Proc. SPIE Int. Soc. Opt. Eng. 6156, 61560Q (2006)
6. For an introduction to the effect of systematic CD variation on electrical performance of pre-90 nm node technology please see: M. Orshansky, L. Milor, and C. Hu; IEEE Transactions on Semiconductor Manufacturing, vol. 17, NO. 1, Feb. 2004, p. 2.
7. For an introduction to across field effects measured electrically and indicating that effects other than physical CD are important please see: M. Babazadeh et al., Proc. SPIE Int. Soc. Opt. Eng. 6155, 615502 (2006)
8. S. Verhaegan et al., Proc. SPIE Int. Soc. Opt. Eng. 6152, 61521Y (2006)
9. S. Talwar, D. Markle, and M. Thompson, Solid-State Technology, July 2003, p. 86
10. Ahsan, I. et al.; 2006 Symposium on VLSI Technology, p. 13-15 June 2006, Honolulu, HI, USA
11. Conference on Advanced Thermal Processing of Semiconductors - RTP2003, J. Gelpey, B. Lojek, Z. Nenyei and R. Singh, Eds., (IEEE, Piscataway, NJ, 2003) p. 17.

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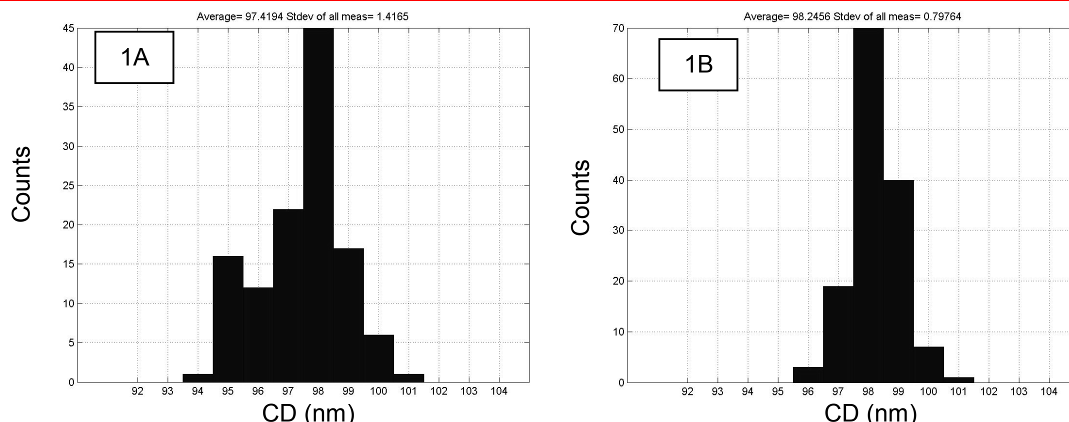

Figure 1. Histograms showing that site to site variation, measured across a scanner field, of the 90 nm node gate CD variation in resist was decreased from a 3 sigma value of 4.2 nm (Figure 1A) early in the technology to less than 2.4 nm (Figure 1B) through mask and process optimization.

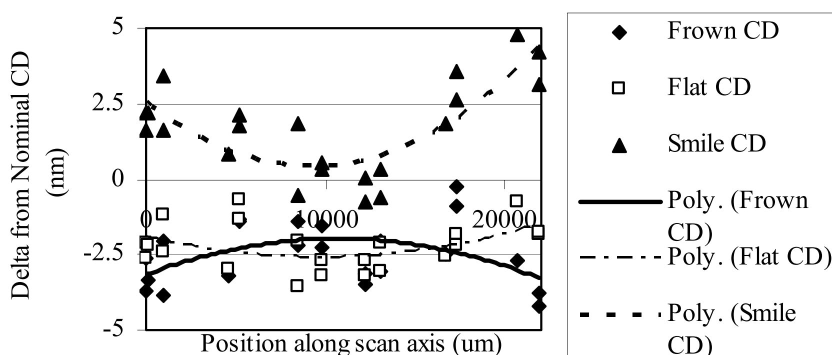

Figure 2. Three different CD signatures across the scan were created by across field dose compensation. The delta from nominal CD reported is an after etch value.

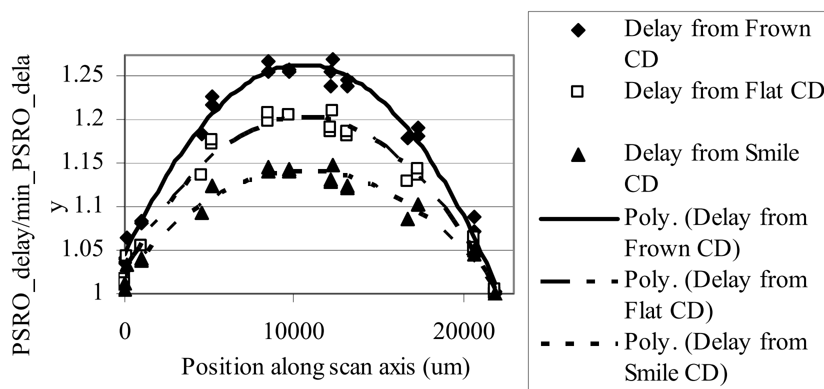

Figure 3. Relative PSRO delay for the three different systematic CD signatures created with dose compensation.

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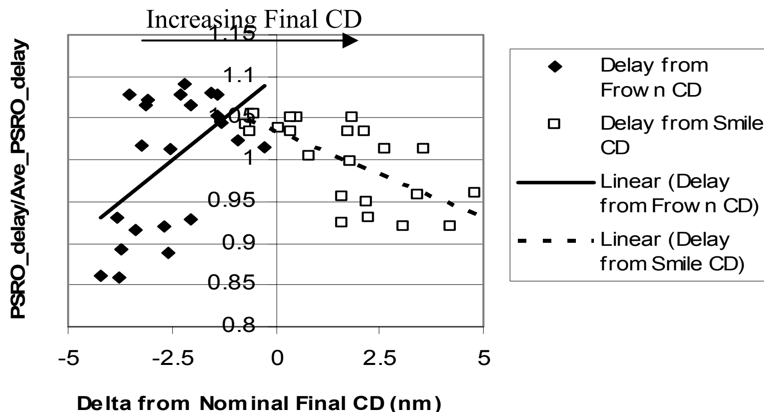

Figure 4. Relationship between relative PSRO delay and final CD for two systematic CD signatures.

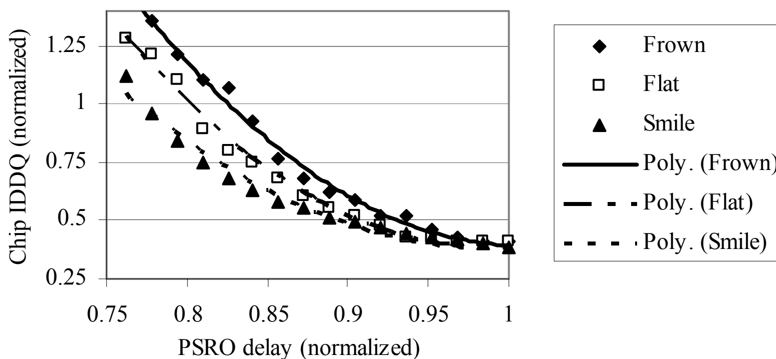

Figure 5. Chip IDDQ as a function of PSRO delay for the three different systematic CD signatures created with dose compensation.

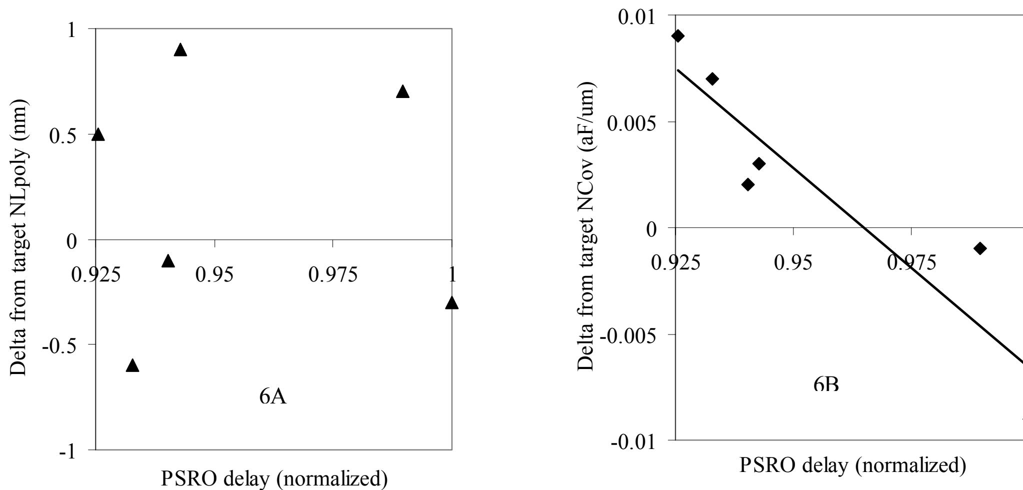

Figure 6. Relationships between PSRO delay and Lpoly (A) and Cov (B).

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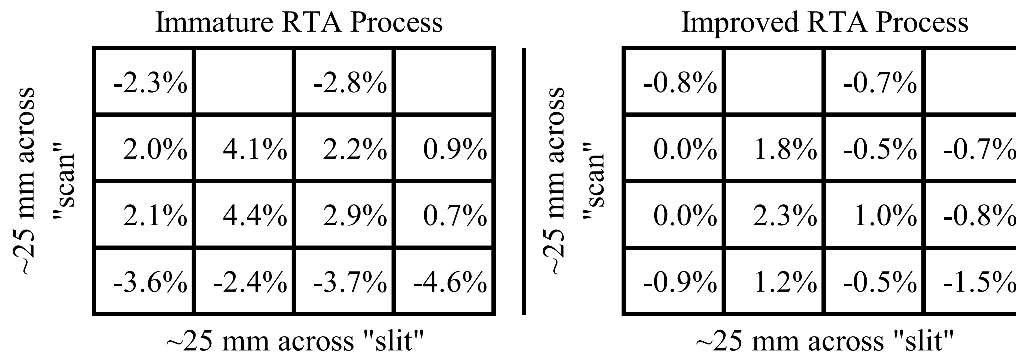
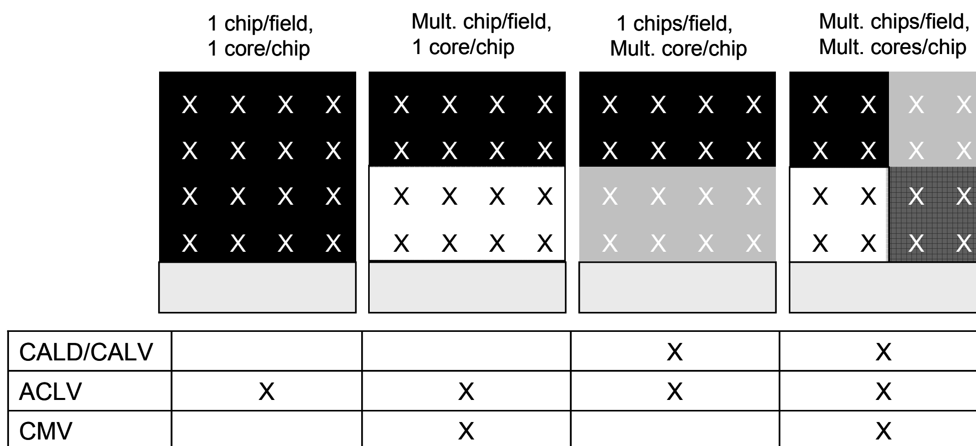


Figure 7. Each field had 14 PSROs placed across it. For the two different anneal types shown the % delta from field's nominal delay is shown.



	1 chip/field, 1 core/chip	Mult. chip/field, 1 core/chip	1 chips/field, Mult. core/chip	Mult. chips/field, Mult. cores/chip
CALD/CALV			X	X
ACLV	X	X	X	X
CMV		X		X

Figure 8. Core average line-width delta (CALD) or variation (CALV) is used to describe a difference in average line-width between cores of a dual or multi core processor respectively. It is differs from ACLV which describes the line-width variation within a chip and chip mean variation (CMV) which describes the variation in the average line-width between chips.

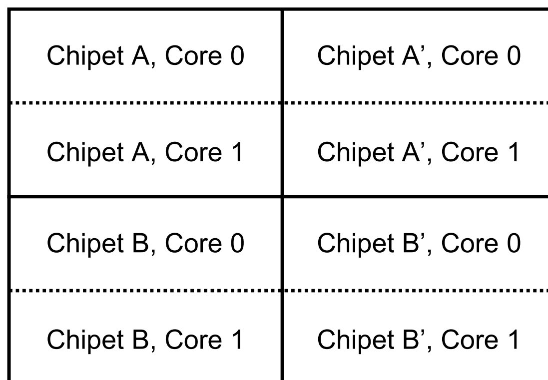


Figure 9. The exposure contains 4 chiplets labeled A, A', B and B'. Each of the chiplets has two cores (core 0 and core 1). Note that chiplets A and A' have core 1 in the interior of the field while chiplets B and B' have core 0 in the interior of the field.

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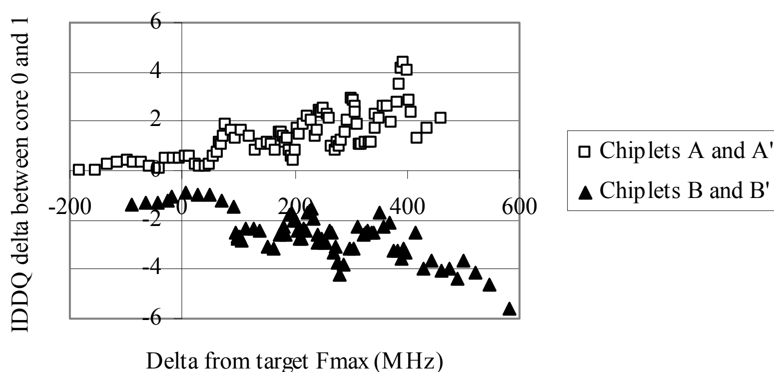

Figure 10. IDDQ delta between two cores in a multicore processor vs. target processor frequency for two different chips within a field.

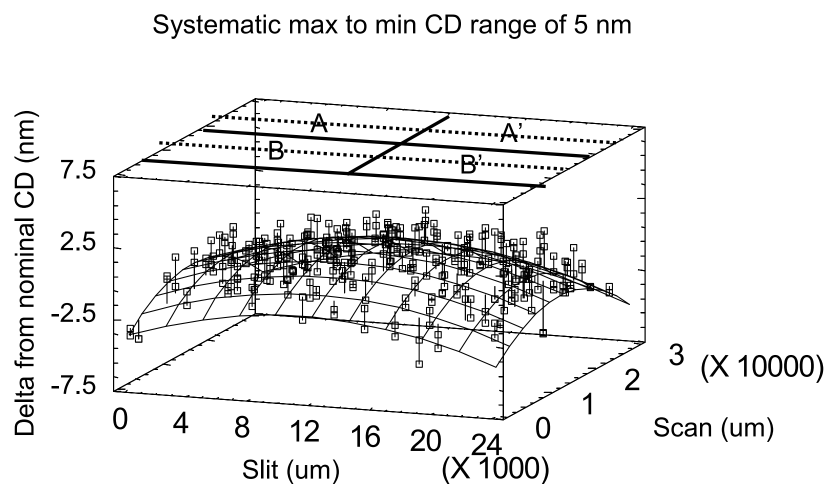

Figure 11. Delta from nominal CD as a function on position within an exposure field. The field's layout and uncorrected spatial CD variation causes the CD of core 0 to be large for chiplets B and B' and small for chiplets A and A'.

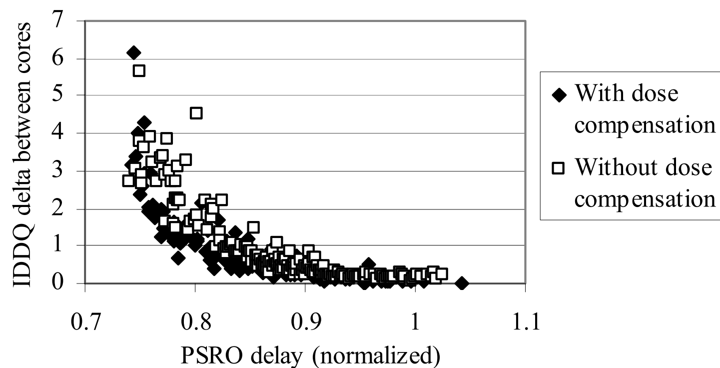

Figure 12. Dose compensation results in a lower IDDQ delta between cores at any given PSRO delay for chip A.

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