In-line non-contact measurement of process induced in-die parametric variability

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Introduction

Metrology axiom[1]: **"***You can't control what you don't measure.***"**

Monitoring and controlling cross-wafer and in-die process induced variability in advanced semiconductor manufacturing has been recognized as an increasingly critical factor for successful commercialization of high-end integrated circuit products[2,3]. The need to complement and manage the critical and yet traditional metrology techniques with parametric-line, in-die measurement that correlate directly to final performance and ultimately (performance) bin yield have been studied[4,5,6]. We have introduced[7] Performance-Based Metrology (PBM) to measure and control variability and to further close the information gap that currently exists between the design, process integration, and manufacturing groups.

The technique scales favorably with advancing technology nodes and it can be applied, after circuit connectivity has been established, from early stages of product development to product ramp, and used as a tool for early predictability of bin-yield and for monitoring across-die, across-wafer, line-to-line, and fab-to-fab product performance.

We present results that demonstrate the technique's usage and potential for early characterization of parametric variability, and give examples of variability induced by gate and patterning related process variations and design-density loads. The system's measurements of in-die final-performance results will be compared to physical metrology measurements.

System and Technology overview

The automated non-contact power activation and measurement system and the associated embedded (in product silicon) test structures (Figure 1) are reviewed.

The on-silicon product-type circuits and components are electrically and functionally independent of the product's circuitry and are drawn from process/design integration and related parametric and metrology libraries[8]. By their design and placement in the active area these test structures exhibit performance sensitivity to process and design-induced variation. The resulting active integrated circuit "targets" do not have the contact pads and the associated overhead circuitry used for traditional parametric contact measurements.

The small footprint of the non-contact structures allow the user to embed test structures in locations of interest across the product active die to measure process/design sensitivity and process induced performance variability at early stages of product development, and ultimately as an integrated part of parametric/metrology systems and measurements used in volume manufacturing.

Sample of Results

Experimental results from PBM measurements on several generations (90, 65, and 45nm) of bulk-Si and SOI product wafers and devices will be presented. Performance based (RO speed) measurement results from non-contact test-structures patterned with varying dose/exposure across the die and wafer, and these results are compared with direct CD measurements. Also results from split lot wafers and associated metrology measurement will be compared with non-contact at-speed measurements from the same active-die and wafers will be presented. Here, as an overview, we present non-contact measurements of in-die variability.

Figure 2 demonstrates the comparison between single site-per-die measurements versus multiple

in-die measurements. The single measurements represent scribe-to-scribe results, whereas the multi-site wafers show in-die variability that is ultimately and directly related to bin-yield. The Figure 3 reports the results of a differential non-contact test structure using two side-by-side ring oscillators, one built with minimum gate length inverters, and the other with longer gate length (~1.7x) inverters. Both ring oscillators were powered from the same non-contact power supply. The differential measurement "nulls" the impact of random local variations so that Leff offset causes a performance difference indicating the magnitude of systematic Leff variations. Figure 3a shows Leff variations across a test wafer, as measured using this technique. Figure 3b shows the histogram of Leff measurements for all devices on the wafer. The measured standard deviation of Leff variations agrees with

average (mean) is the same between the two measurements, where as the distribution of the results show a 75% increase in variability.

the expected gate CD variations as given in the process specification.

Figure 1: PBM system architecture

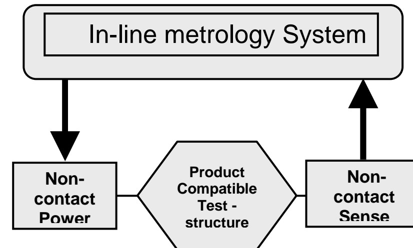


Figure 2: Comparison of Cross-wafer vs. Cross-die Variability

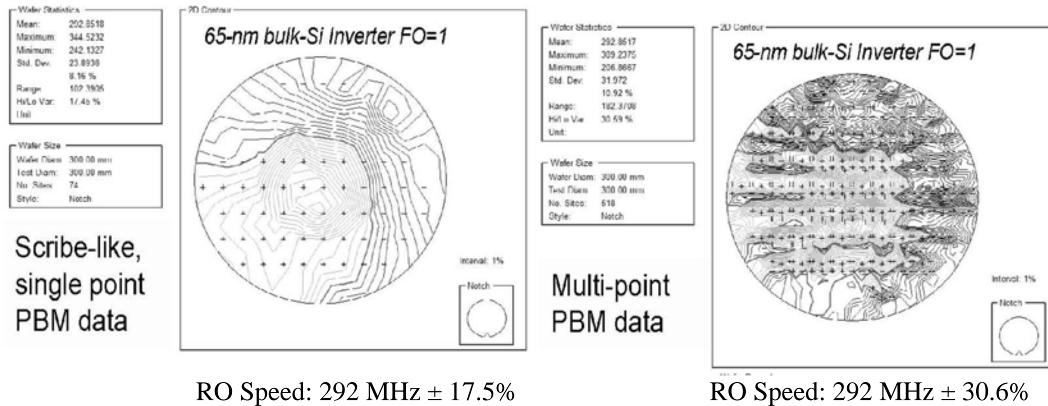
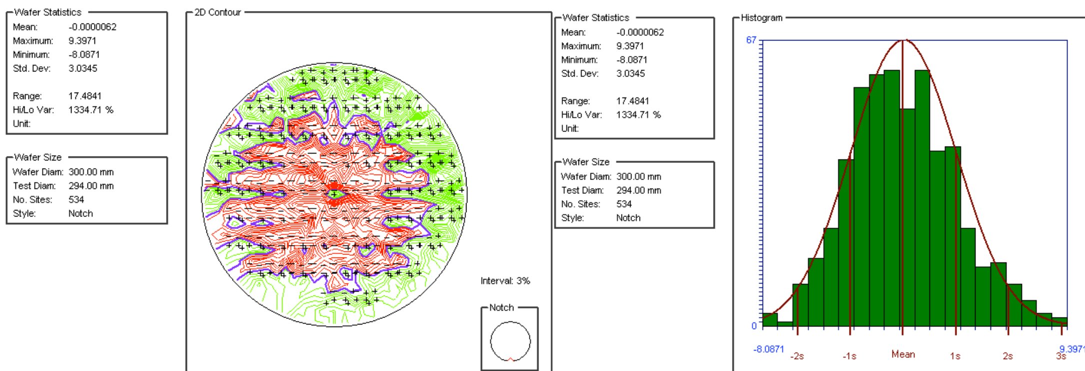


Figure 3: Cross-wafer and Cross-die L_{eff} Variability



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1 Anonymous.

2 Kelin J. Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Wei-kai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, and Keith Zawadzki, "Managing Porcess Varaition in Intel's 45nm CMOS Technology", *Intel technology Journal*, vol.12, no.2, pp. 93-109, 2008

[3] Duane S. Boning, Karthik Balakrishnan, Hong Cai, Nigel Drego, Ali Farahanchi, Karen Gettings, Daihyun Lim, Ajay Somani, Hayden Taylor, Daniel Truque, Xiaolin Xie, “Variation”, *Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED) 2007,* pp. 15-20.

[4] A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N. Le, P. Lindo, A. P. Mahorowala, H.-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas and H. Utomo, “Improving the Power-Performance of Multicore Processors Through Optimization of Lithography and Thermal Processing”, *Proc. of SPIE,* vol. 6521, pp. 65210K, 2007.

[5] B. Nikolic, L.T. Pang, "Measurements and analysis of process variability in 90nm CMOS, " *Proc. 8th International Conference on Solid-State and Integrated Circuit Technology*, Shanghai, China, October 23-26, 2006. (invited), pp. 505-508..

[6] Sharad Saxena, Christopher Hess, Hossein Karbasi, Angelo Rossoni, Stefano Tonello, Patrick McNamara, Silvia Lucherini, Seán Minehane, Christoph Dolainsky, and Michele Quarantelli, “Variation in Transistor Performance and Leakage in Nanometer-Scale Technologies”, IEEE *TRANSACTIONS ON ELECTRON DEVICES*, vol. 55, no. 1, pp. 131-143, Jan. 2008.

[7] Majid Babazadeh, Bertrand Borot, Wim Doedel, José Estabil, Jean Galvier, Gloria Johnson, Nader Pakdaman, Gary Steinbrueck, and James Vickers, “First Look at Across-chip Performance Variation Using Non-Contact, Performance-Based Metrology”; *17th Annual SEMI/IEEE* Advanced Semiconductor Manufacturing Conference, (ASMC 2006), pp. 278-283.

[8] Mark B. Ketchen, Manjul Bhushan, “Product-representative 'at speed' test structures for CMOS characterization”, *IBM Journal of Research and Development, vol. 50*, no. 4/5, pp. 451-468, 2006.